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JALB0 Schematics Document

AMD Griffin Processor with RS780M+SB700

(With ATI MXM/B)

2008-8-14

REV:2.0

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				Date: Thursday, August 14, 2008; Sheet 1 of 50

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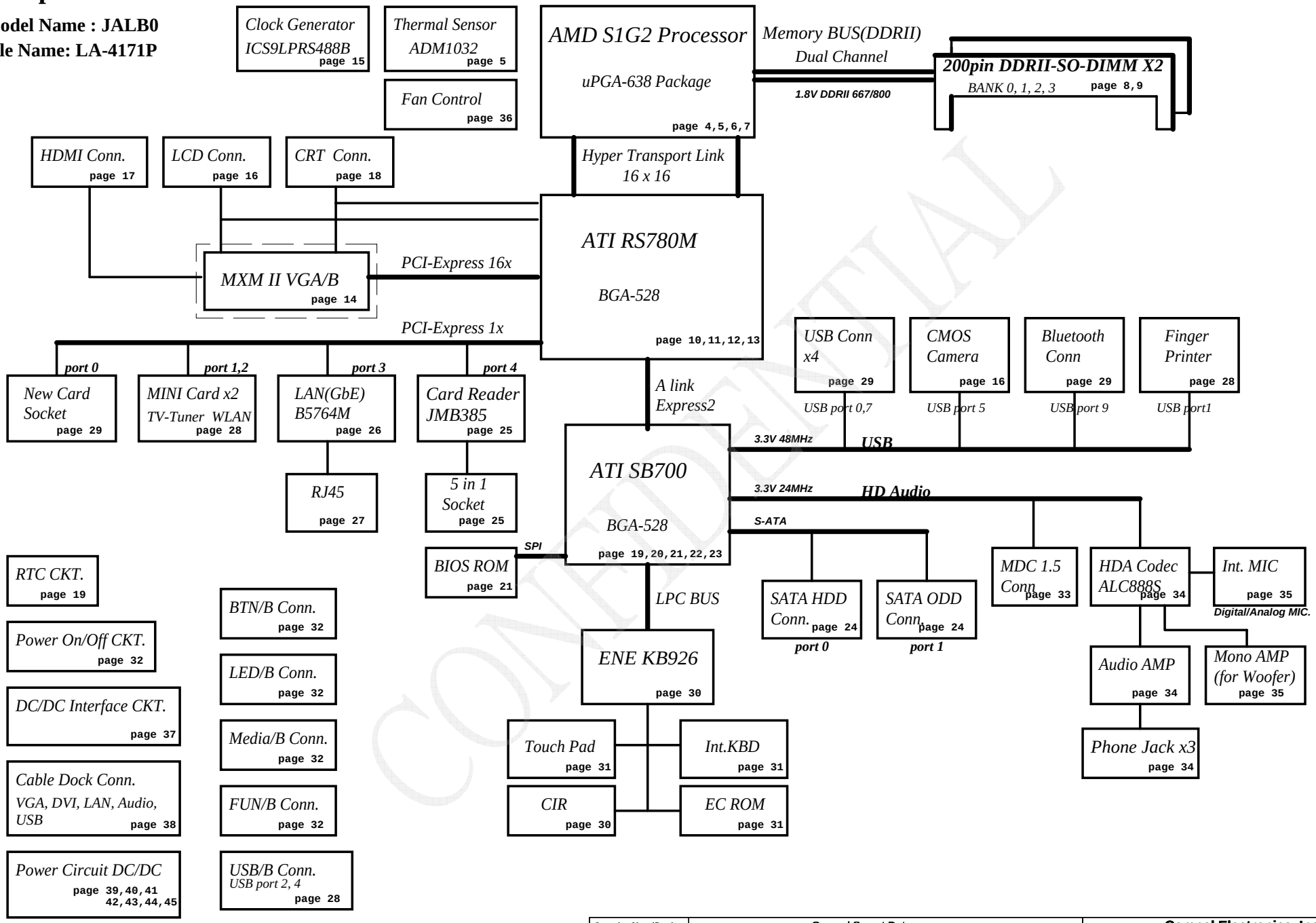
Model Name : JALB0
File Name: LA-4171P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE_0	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_NB	Core voltage for CPU	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.05V switched power rail	ON	OFF	OFF
+1.2V_HT	1.25V switched power rail	ON	OFF	OFF
+NB_CORE	1.0V~1.1V switched power rail for NB VDDC	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.8V	1.8V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA and MXM/B	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

No PCI device

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
MXM GMT G781-1	1001 101X b

EC SM Bus2 address

Device	Address
ADI ADM1032	1001 100X b
CPU SB	1001 101X b

SB700 SM Bus 0 address

Device	Address
Clock Generator (ICS9LPRS365)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
Minicard	
Minicard	

SB700 SM Bus 1 address

Device	Address
New card	
Lan	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
* 2	0.3 0.4 1.0
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
Discrete	VGA@
UMA	UMA@

PROJECT ID Table

Board ID	PROJECT
0	JALB0
1	JALC0
2	
3	
4	
5	
6	
7	

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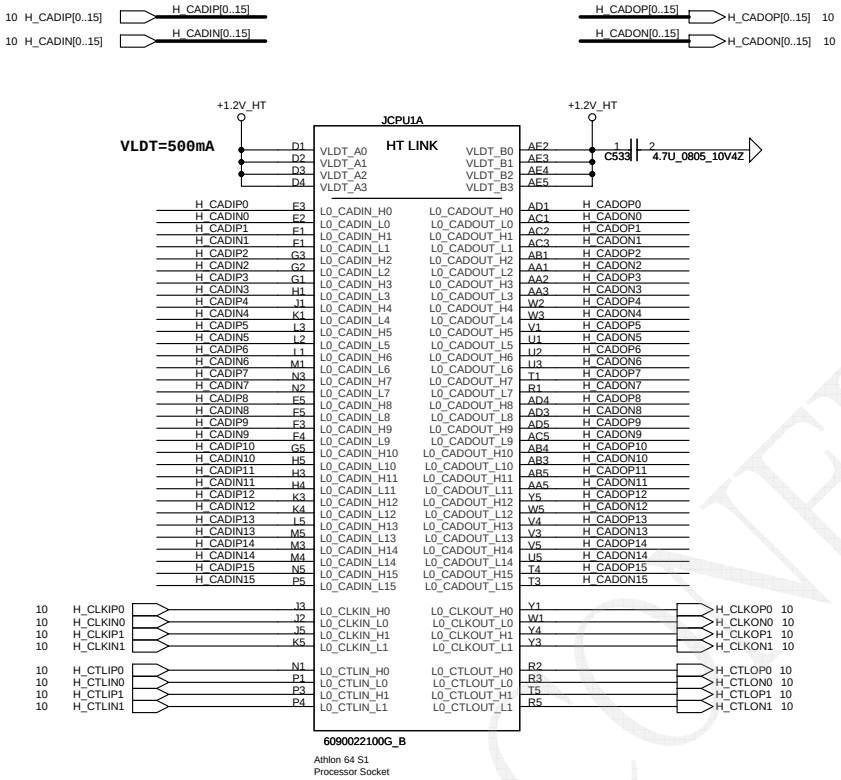

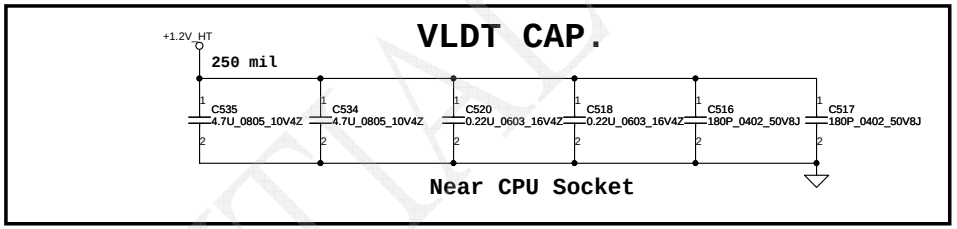

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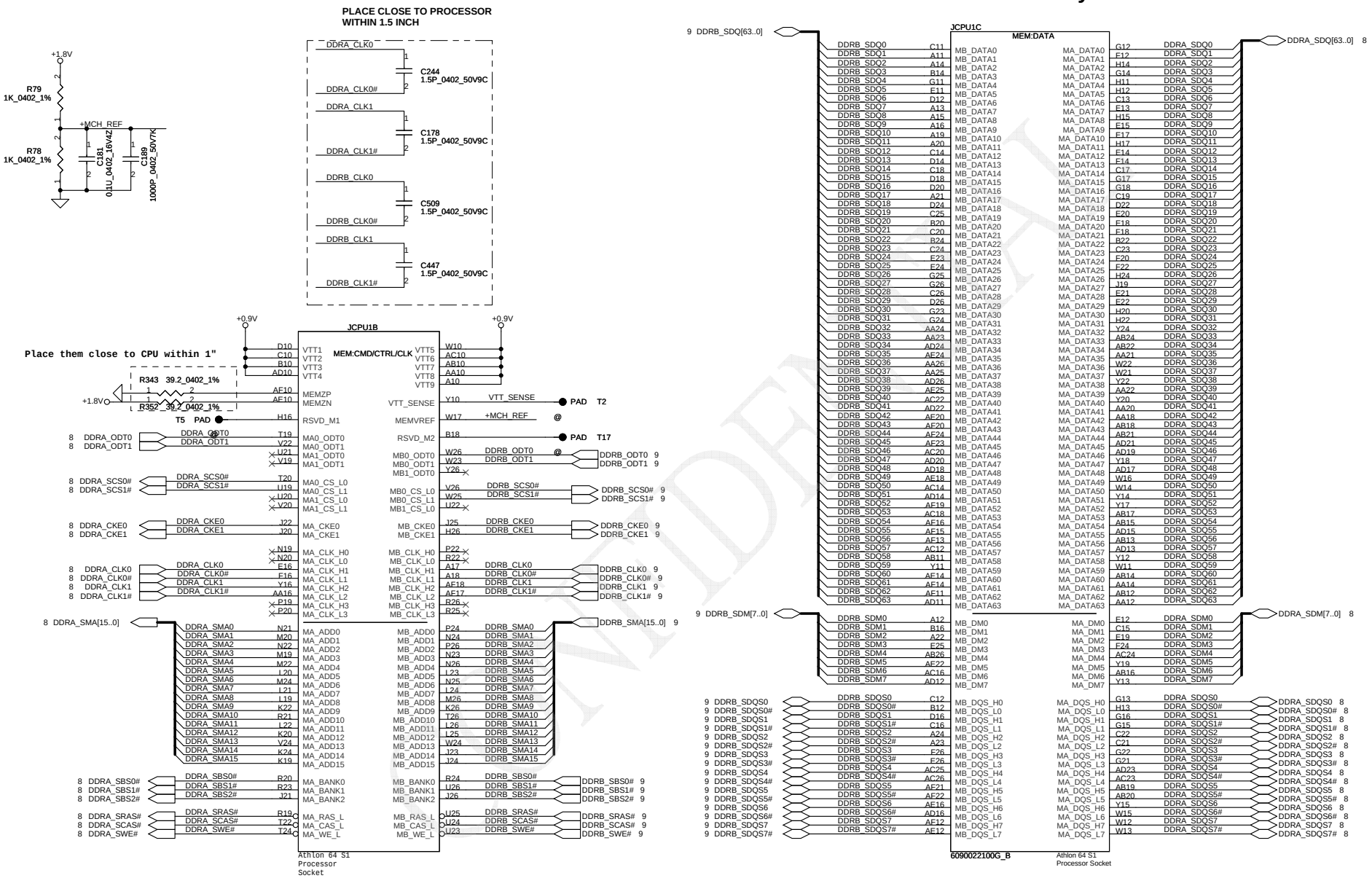
Processor DDR2 Memory Interface



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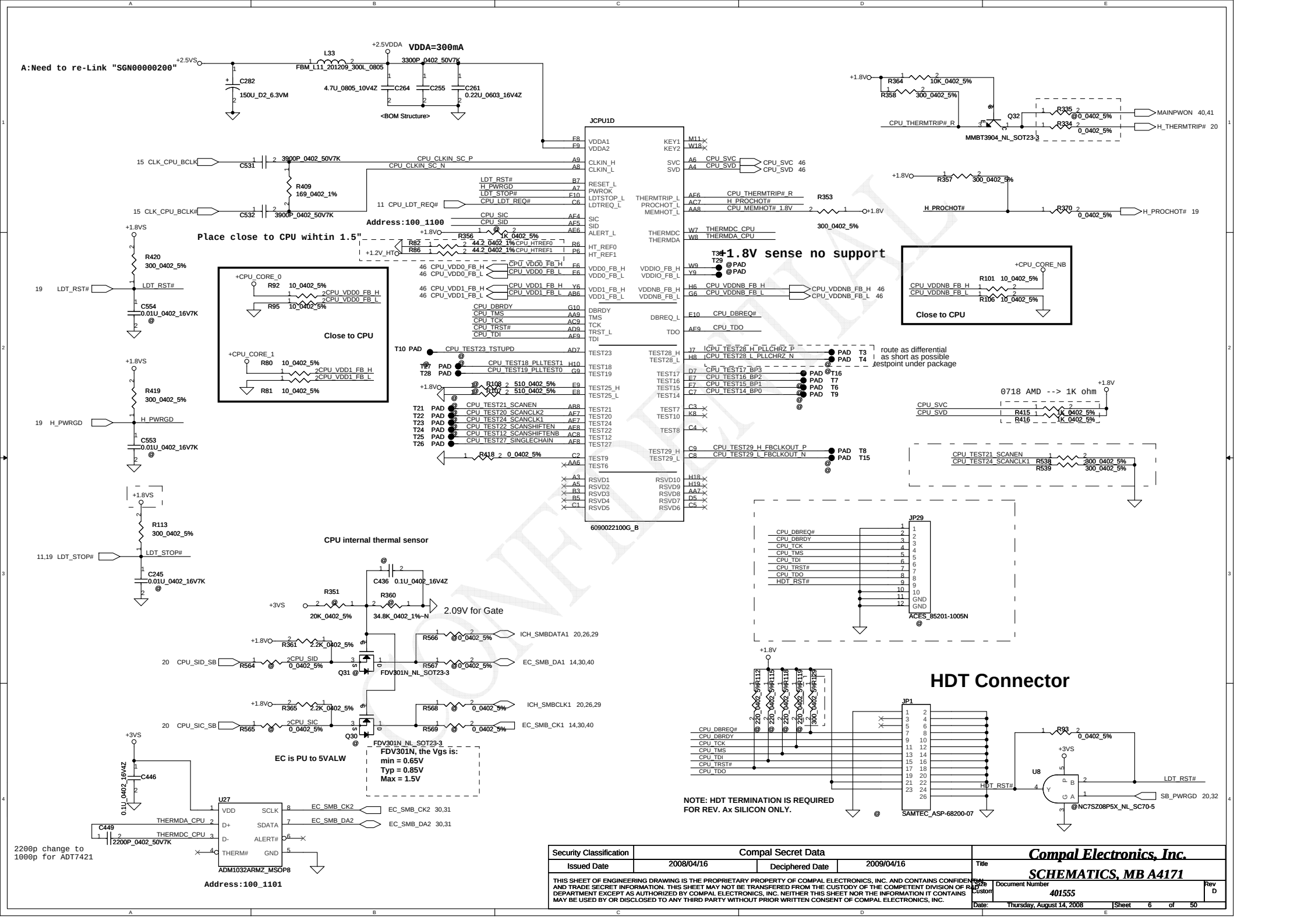

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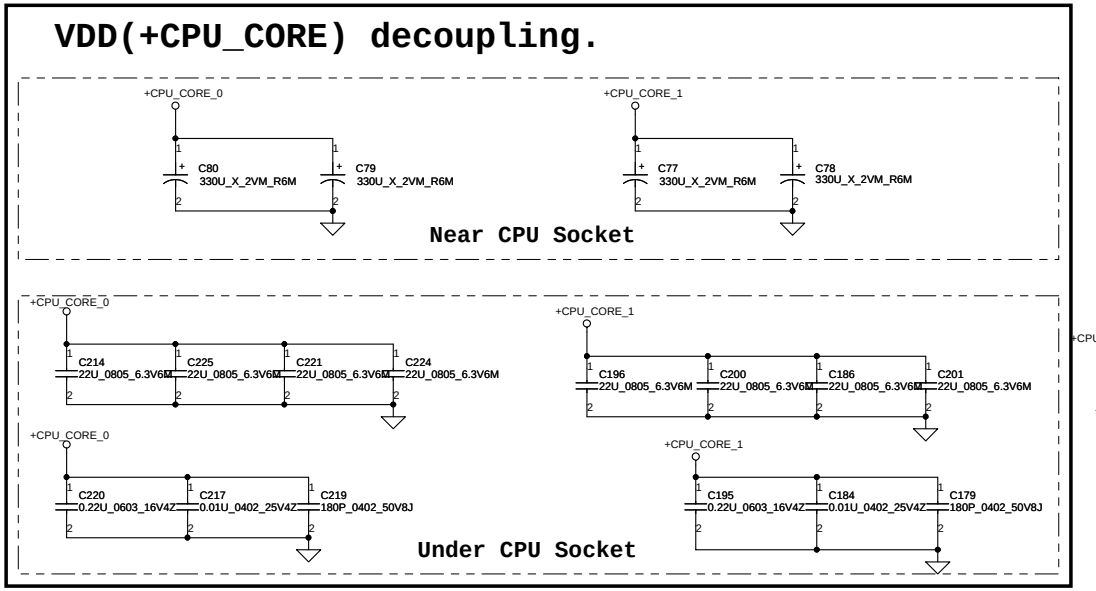
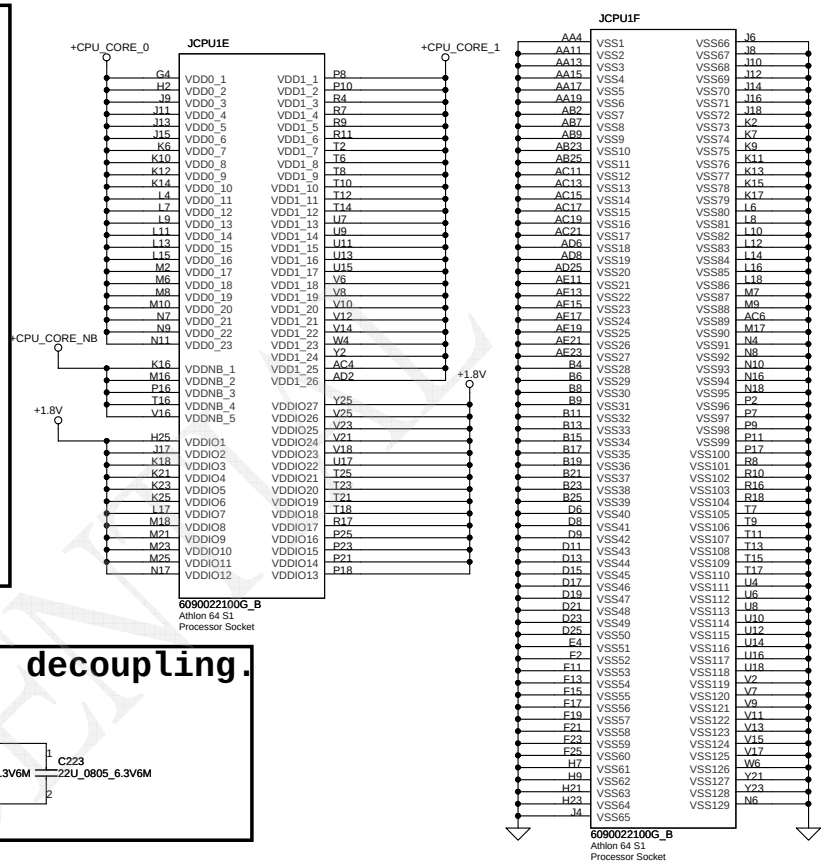
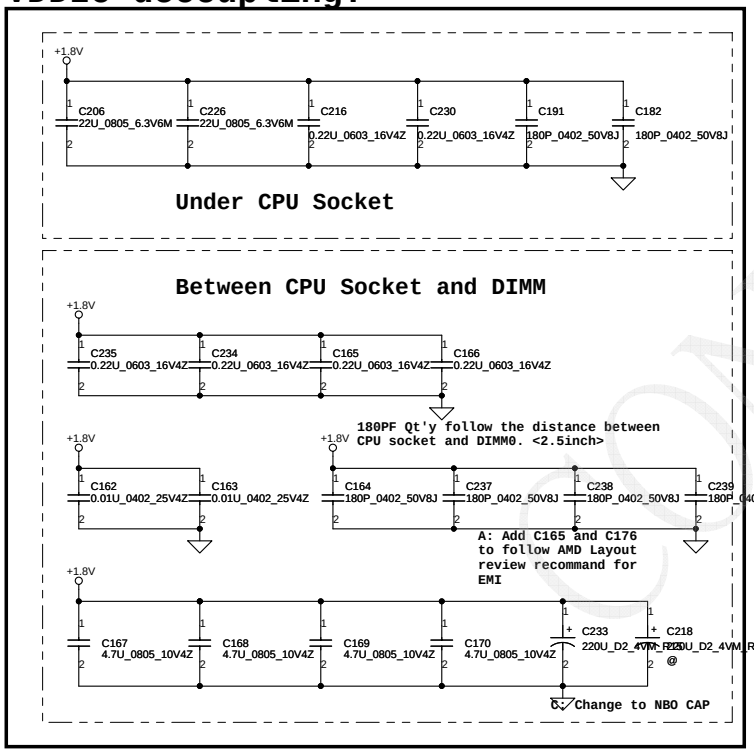
VDD(+CPU_CORE) decoupling.

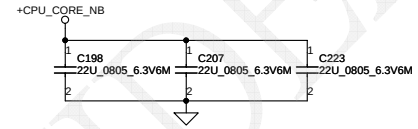




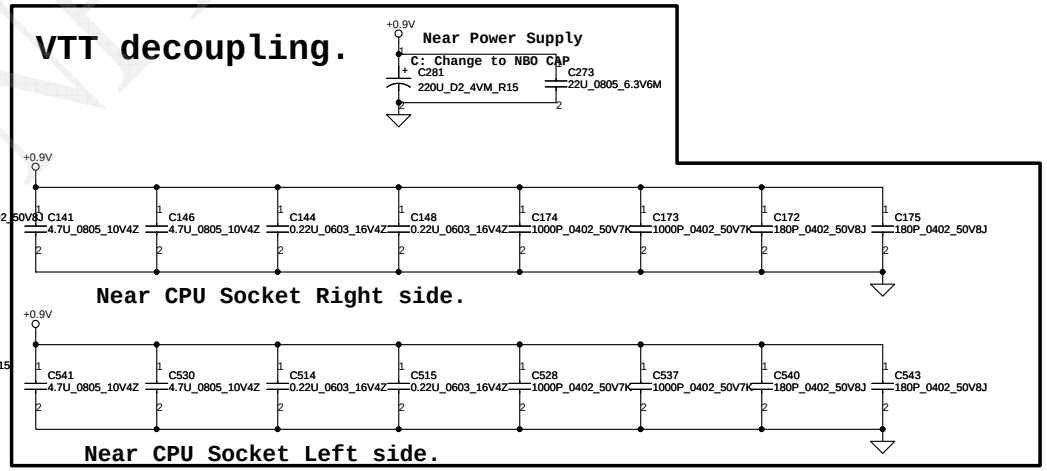
VDDIO decoupling.



+CPU_CORE_NB decoupling.



VTT decoupling.



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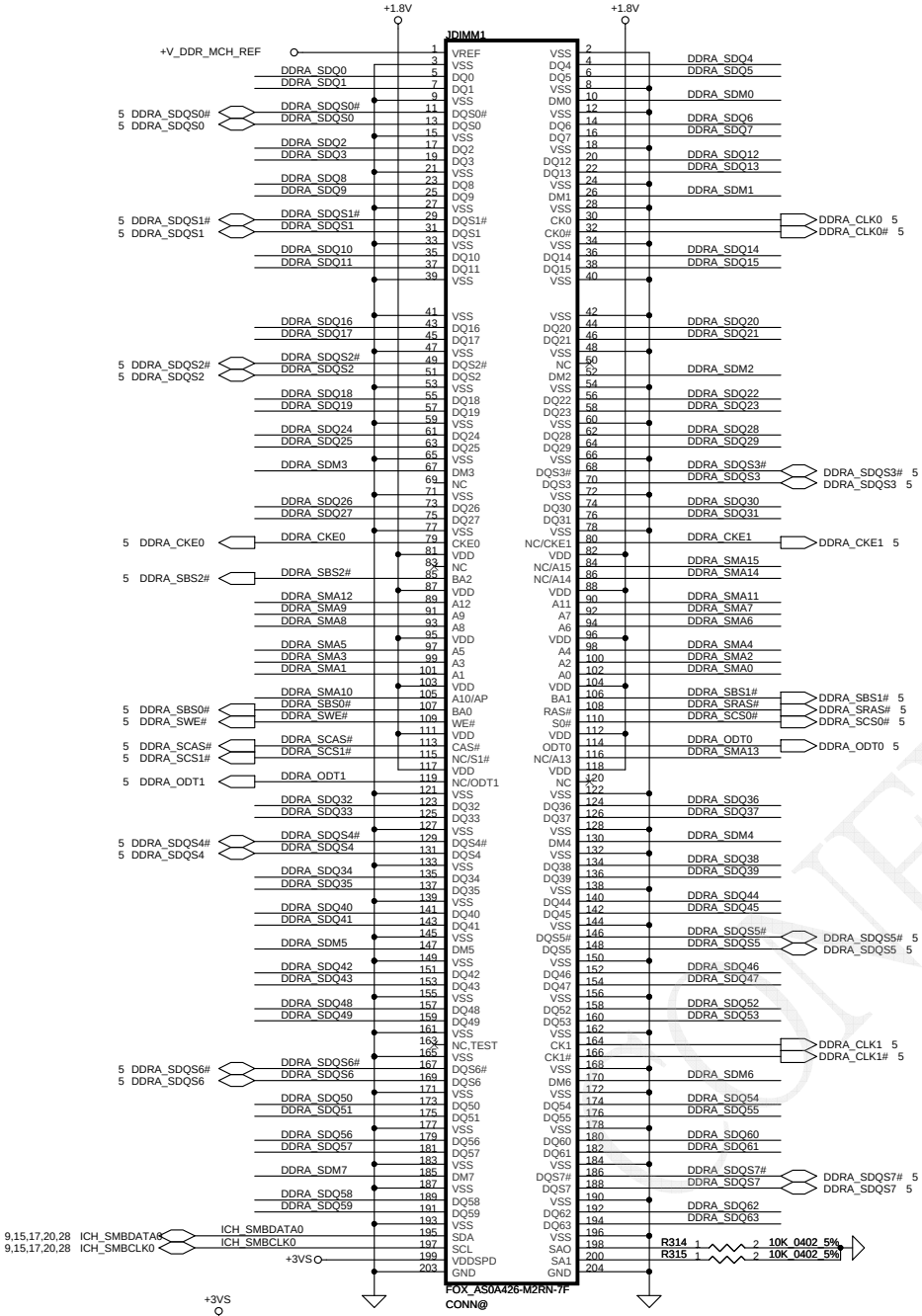
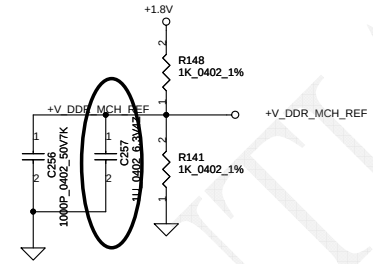
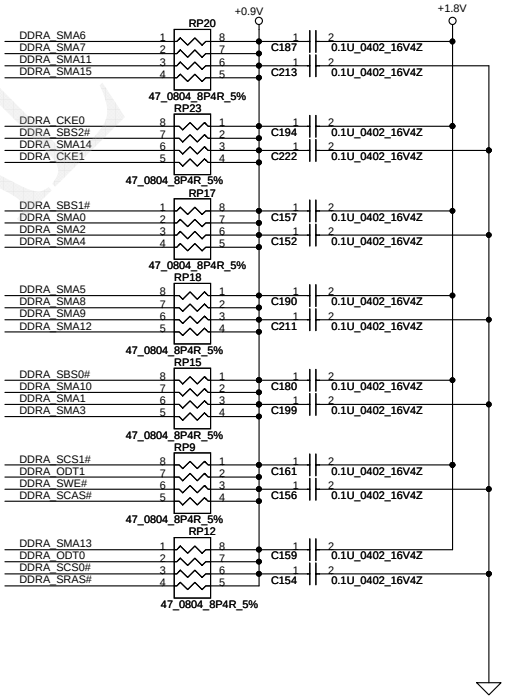
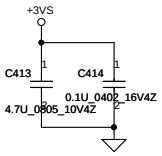
RESERVE
+V_DDR_MCH_REF BUFFER CIRCUIT









DIMM1 REV H:5.2mm (BOT)

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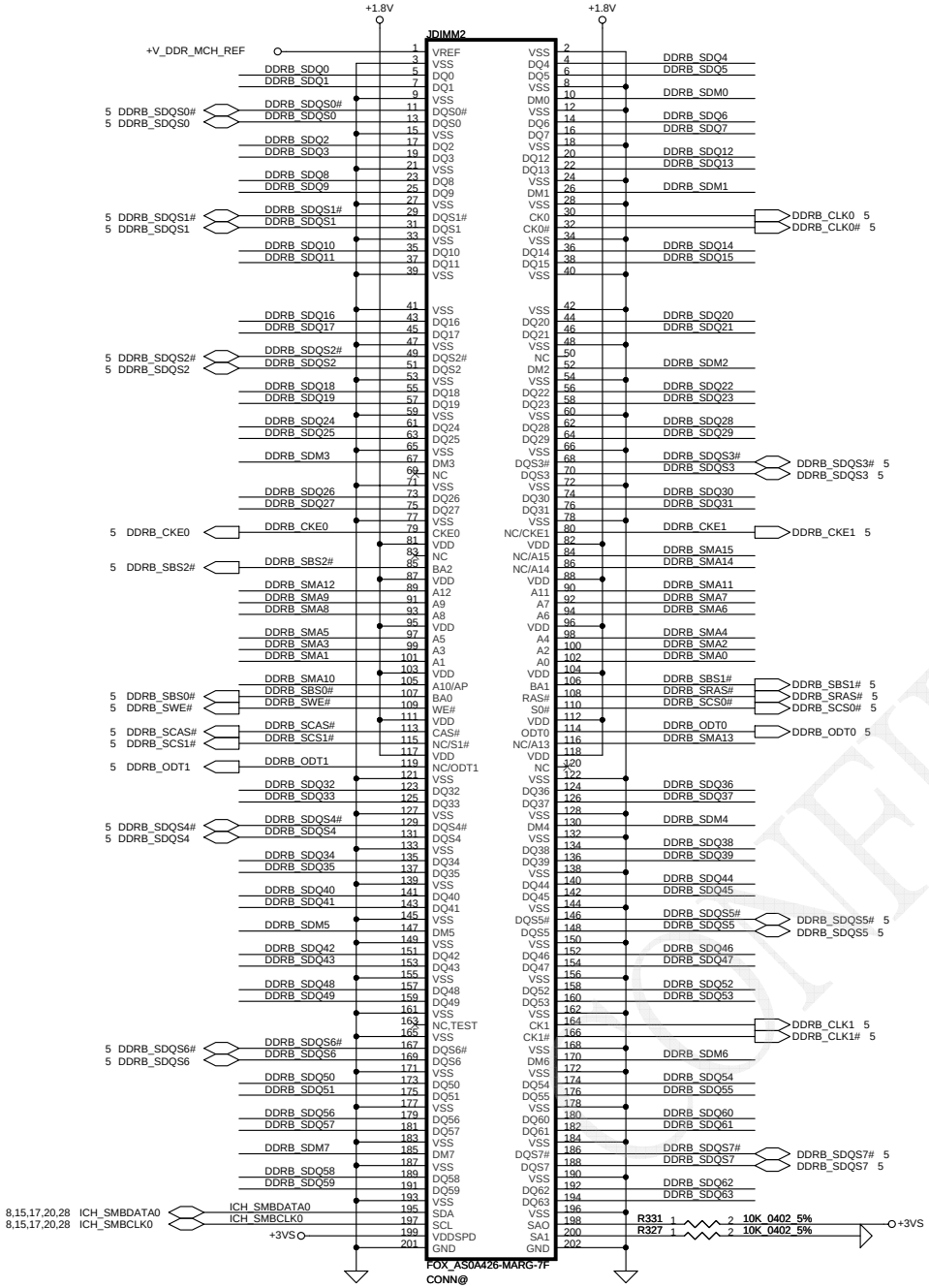

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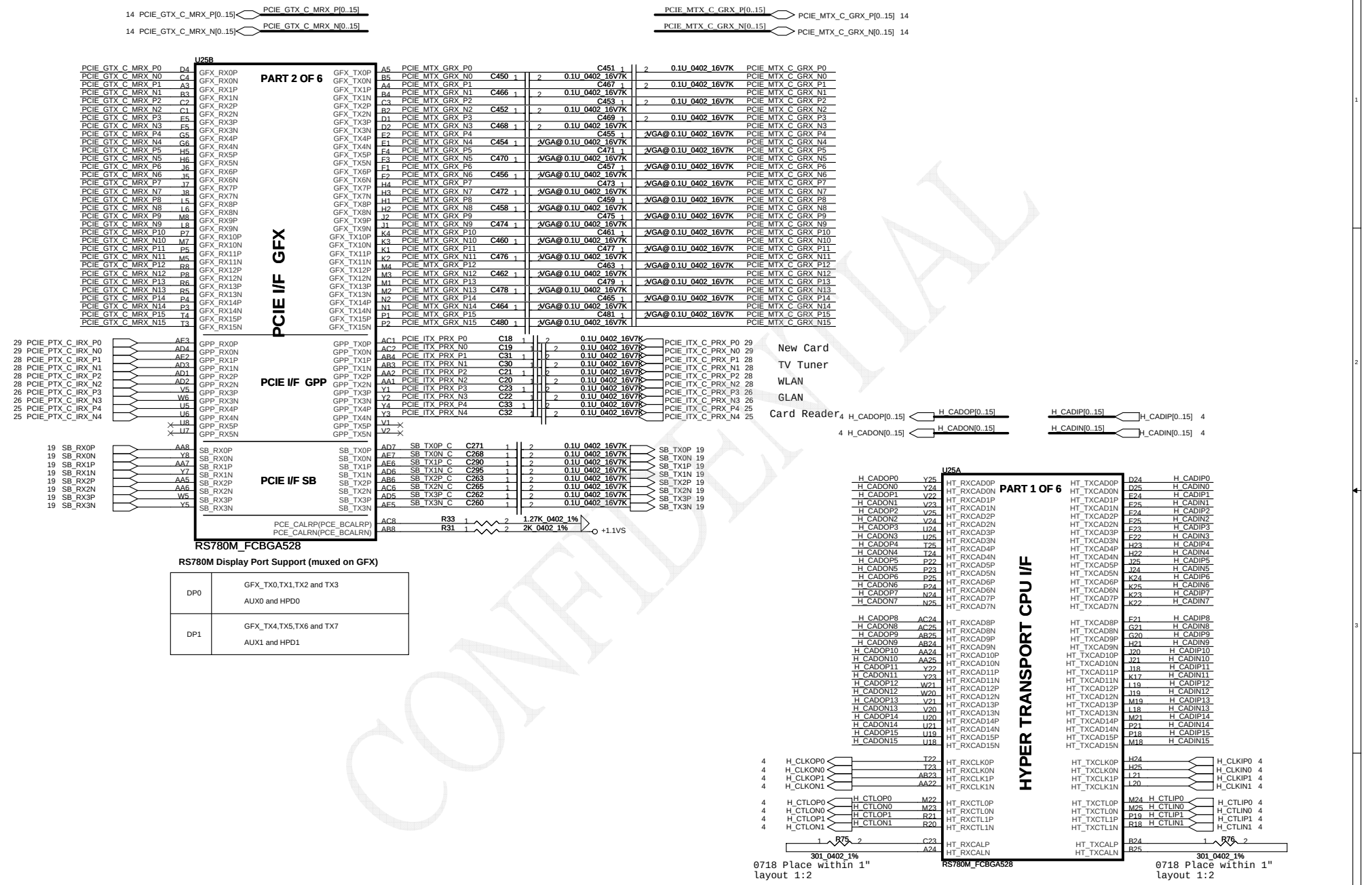

RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

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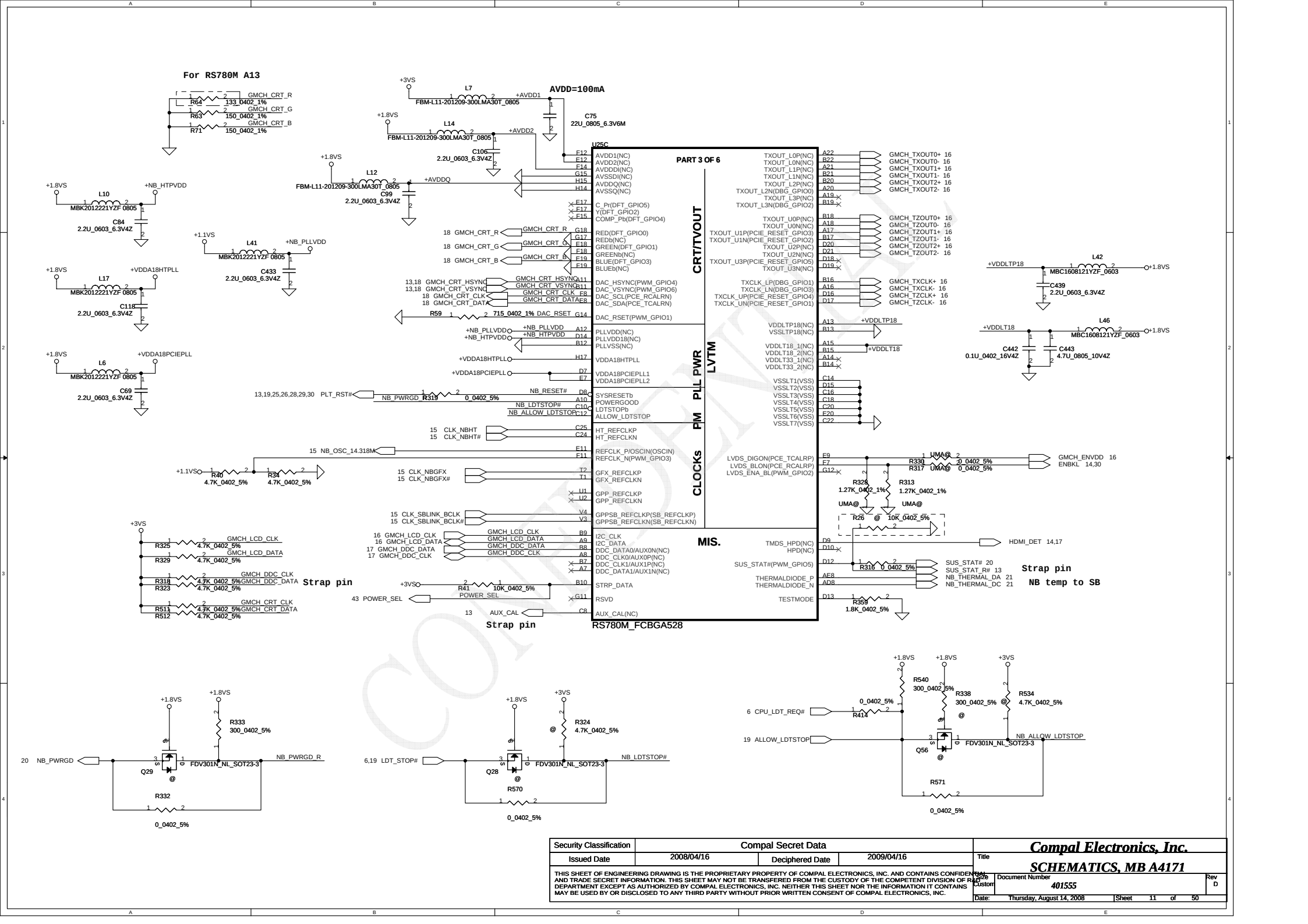

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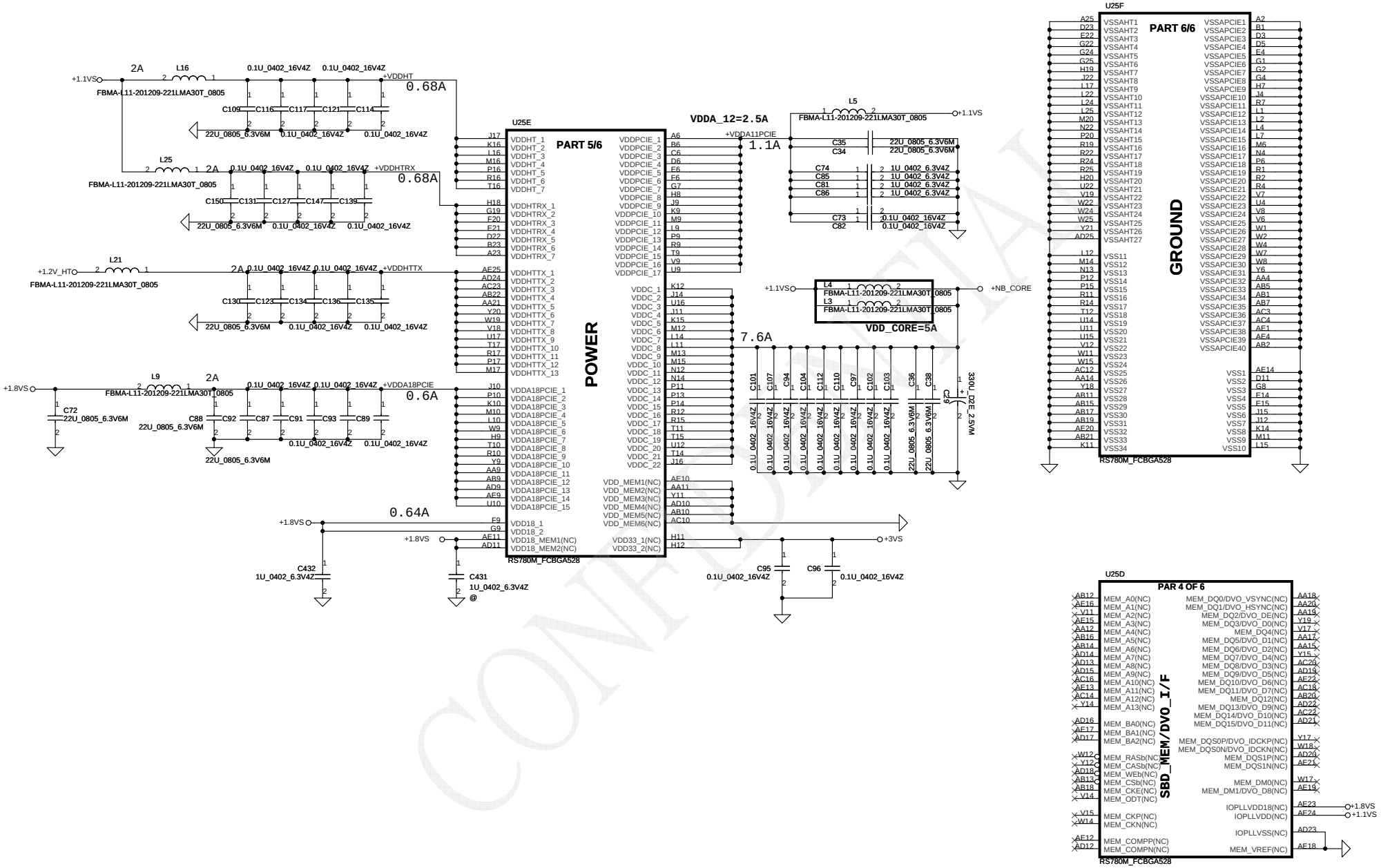

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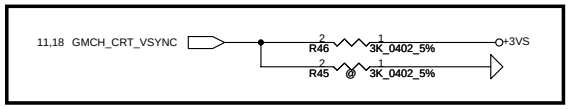
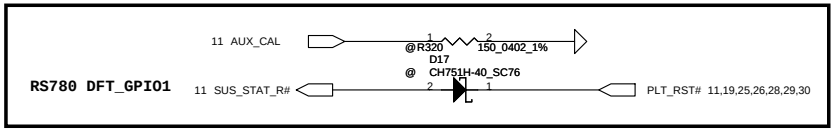


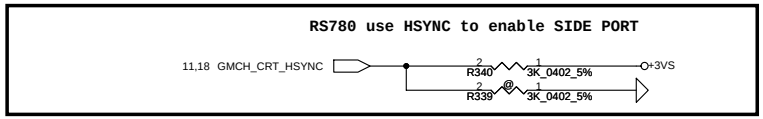
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

```
Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable (RS780)
0 : Enable (Rs780)
```



DFT_GPIO1: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS740/RX780: DFT_GPIO1  RS780:SUS_STAT
```



RS780 use HSYNC to enable SIDE PORT

```
RS740/RS780: Enables Side port memory ( RS780 use HSYNC#)
0.   Enable (RS780)
1 :  Disable(RS780)
```

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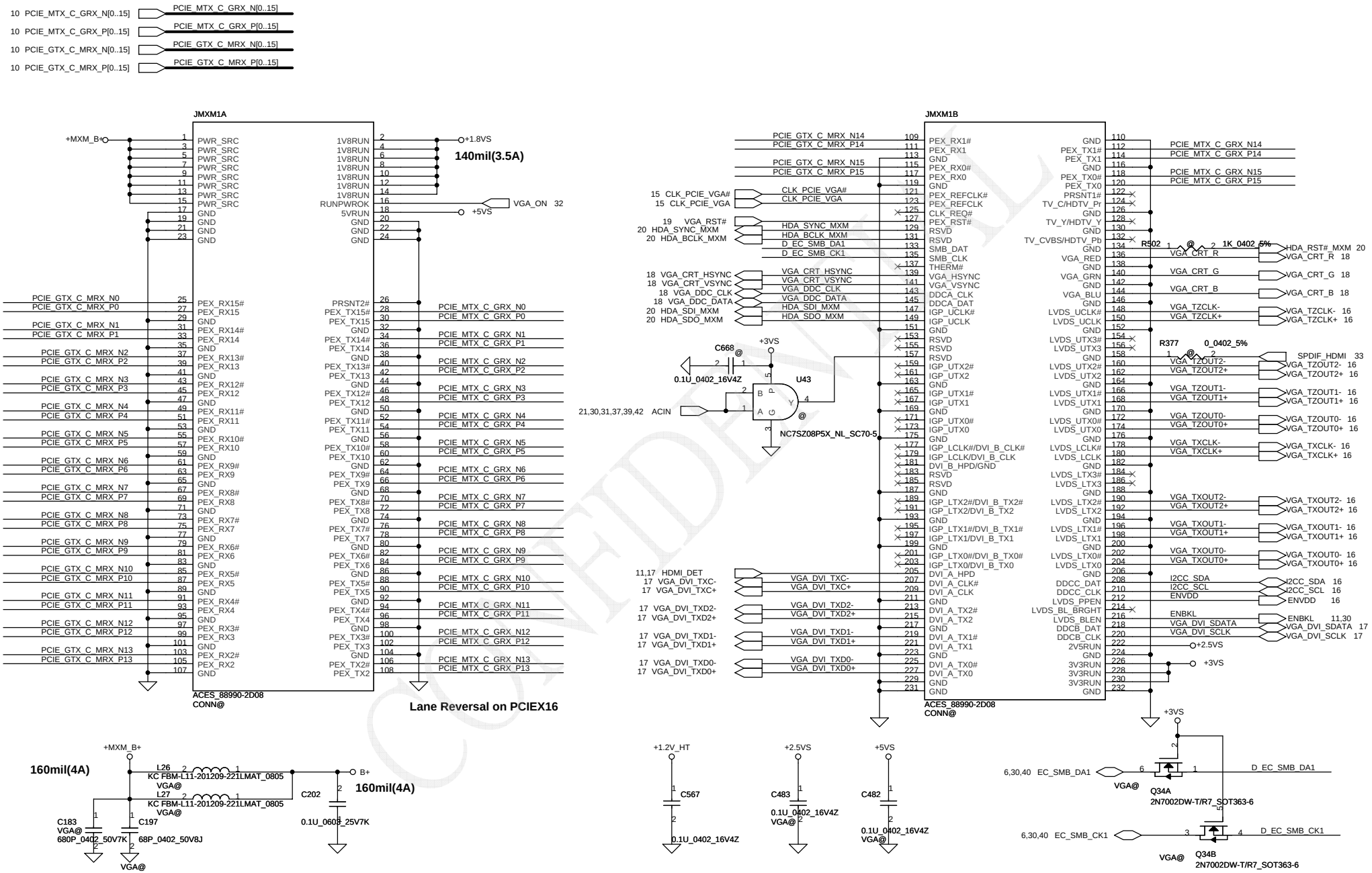

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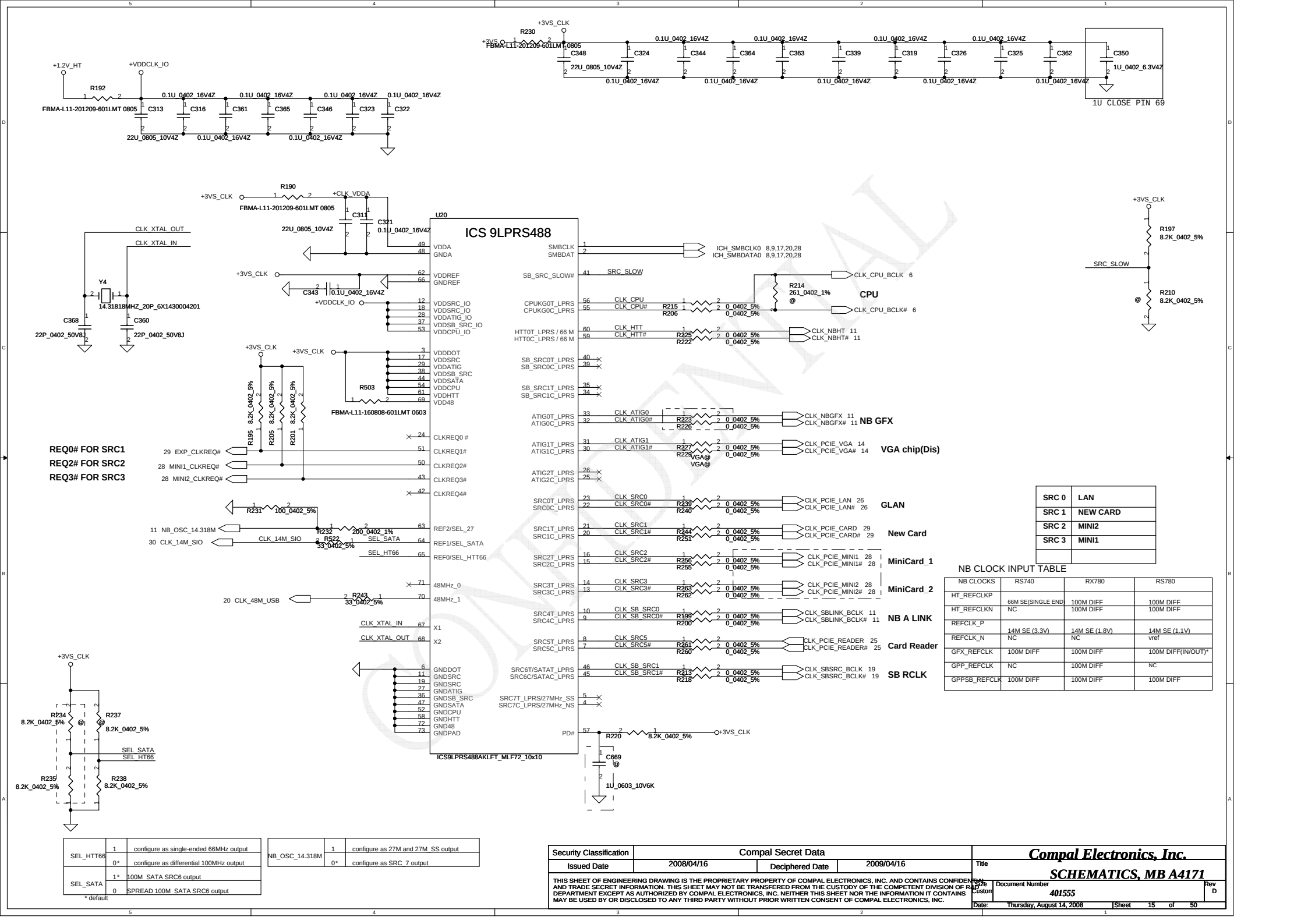
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ICS9LPRS488AKLFT_MLF72_10x10
+3VS_CLK
+1.2V_HT
+VDDCLK_IO
+CLK_VDDA
R192
FBMA-L11-201209-601LMT 0805
R190
R230
0.1U_0402_16V4Z
22U_0805_10V4Z
1U CLOSE PIN 69
1U_0402_6.3V4Z
CLK_XTAL_OUT
CLK_XTAL_IN
Y4
14.31818MHZ_20P_6X1430004201
C368
22P_0402_50V8J
C360
22P_0402_50V8J
R503
FBMA-L11-160808-601LMT 0603
R195 8.2K_0402_5%
R205 8.2K_0402_5%
R201 8.2K_0402_5%
REQ0# FOR SRC1
REQ2# FOR SRC2
REQ3# FOR SRC3
29 EXP_CLKREQ#
28 MINI1_CLKREQ#
28 MINI2_CLKREQ#
R231 100_0402_5%
11 NB_OSC_14.318M
30 CLK_14M_SIO
R232 200_0402_1%
R222 33_0402_5%
SEL_SATA
SEL_HT66
20 CLK_48M_USB
R243 33_0402_5%
R234 8.2K_0402_5%
R237 8.2K_0402_5%
R235 8.2K_0402_5%
R238 8.2K_0402_5%
SMBCLK
SMBDAT
ICH_SMBCLK0 8,9,17,20,28
ICH_SMBDATA0 8,9,17,20,28
SB_SRC_SLOW#
SRC_SLOW
R197 8.2K_0402_5%
R210 8.2K_0402_5%
CPUKG0T_LPRS
CPUKG0C_LPRS
CLK_CPU
CLK_CPU#
R215 261_0402_1%
R206 0_0402_5%
R214 261_0402_1%
CLK_CPU_BCLK 6
CLK_CPU_BCLK# 6
CPU
HTT0T_LPRS / 66 M
HTT0C_LPRS / 66 M
CLK_HTT
CLK_HTT#
R225 0_0402_5%
R222 0_0402_5%
CLK_NBHT 11
CLK_NBHT# 11
SB_SRC0T_LPRS
SB_SRC0C_LPRS
SB_SRC1T_LPRS
SB_SRC1C_LPRS
ATIG0T_LPRS
ATIG0C_LPRS
CLK_ATIG0
CLK_ATIG0#
R223 0_0402_5%
R226 0_0402_5%
CLK_NBGFX 11
CLK_NBGFX# 11
NB GFX
ATIG1T_LPRS
ATIG1C_LPRS
CLK_ATIG1
CLK_ATIG1#
R227 0_0402_5%
R228 0_0402_5%
VGA@
CLK_PCIE_VGA 14
CLK_PCIE_VGA# 14
VGA chip(Dis)
ATIG2T_LPRS
ATIG2C_LPRS
SRC0T_LPRS
SRC0C_LPRS
CLK_SRC0
CLK_SRC0#
R239 0_0402_5%
R240 0_0402_5%
CLK_PCIE_LAN 26
CLK_PCIE_LAN# 26
GLAN
SRC1T_LPRS
SRC1C_LPRS
CLK_SRC1
CLK_SRC1#
R244 0_0402_5%
R251 0_0402_5%
CLK_PCIE_CARD 29
CLK_PCIE_CARD# 29
New Card
SRC2T_LPRS
SRC2C_LPRS
CLK_SRC2
CLK_SRC2#
R256 0_0402_5%
R255 0_0402_5%
CLK_PCIE_MINI1 28
CLK_PCIE_MINI1# 28
MiniCard_1
SRC3T_LPRS
SRC3C_LPRS
CLK_SRC3
CLK_SRC3#
R263 0_0402_5%
R262 0_0402_5%
CLK_PCIE_MINI2 28
CLK_PCIE_MINI2# 28
MiniCard_2
SRC4T_LPRS
SRC4C_LPRS
CLK_SB_SRC0
CLK_SB_SRC0#
R199 0_0402_5%
R200 0_0402_5%
CLK_SBLINK_BCLK 11
CLK_SBLINK_BCLK# 11
NB A LINK
SRC5T_LPRS
SRC5C_LPRS
CLK_SRC5
CLK_SRC5#
R261 0_0402_5%
R260 0_0402_5%
CLK_PCIE_READER 25
CLK_PCIE_READER# 25
Card Reader
SRC6T/SATAT_LPRS
SRC6C/SATAC_LPRS
CLK_SB_SRC1
CLK_SB_SRC1#
R213 0_0402_5%
R218 0_0402_5%
CLK_SBSRC_BCLK 19
CLK_SBSRC_BCLK# 19
SB RCLK
SRC7T_LPRS/27MHz_SS
SRC7C_LPRS/27MHz_NS
PD#
R220 8.2K_0402_5%
C669
1U_0603_10V6K
VDDA
GNDA
VDDREF
GNDREF
VDDSRC_IO
VDDATIG_IO
VDDSB_SRC_IO
VDDCPU_IO
VDDDOT
VDDSRC
VDDATIG
VDDSB_SRC
VDDSATA
VDDCPU
VDDHTT
VDD48
CLKREQ0 #
CLKREQ1#
CLKREQ2#
CLKREQ3#
CLKREQ4#
REF2/SEL_27
REF1/SEL_SATA
REF0/SEL_HTT66
48MHz_0
48MHz_1
X1
X2
GNDDOT
GNDSRC
GNDATIG
GNDSB_SRC
GNDSATA
GNDCPU
GNDHTT
GND48
GNDPAD
SEL_HTT66
1 configure as single-ended 66MHz output
0* configure as differential 100MHz output
SEL_SATA
1* 100M SATA SRC6 output
0 SPREAD 100M SATA SRC6 output
* default
NB_OSC_14.318M
1 configure as 27M and 27M_SS output
0* configure as SRC_7 output
SRC 0 LAN
SRC 1 NEW CARD
SRC 2 MINI2
SRC 3 MINI1
NB CLOCK INPUT TABLE
NB CLOCKS RS740 RX780 RS780
HT_REFCLKP 66M SE(SINGLE END) 100M DIFF 100M DIFF
HT_REFCLKN NC 100M DIFF 100M DIFF
REFCLK_P 14M SE (3.3V) 14M SE (1.8V) 14M SE (1.1V)
REFCLK_N NC NC vref
GFX_REFCLK 100M DIFF 100M DIFF 100M DIFF(IN/OUT)*
GPP_REFCLK NC 100M DIFF NC
GPPSB_REFCLK 100M DIFF 100M DIFF 100M DIFF
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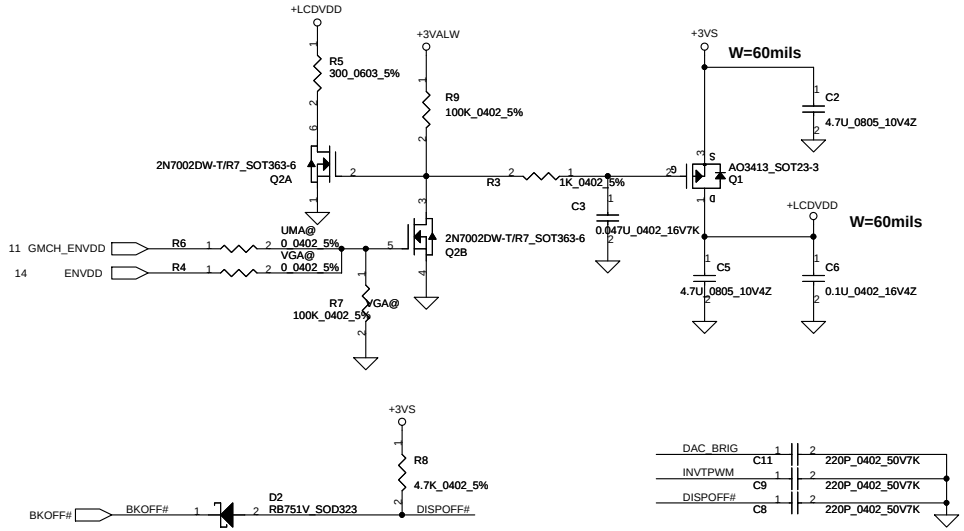
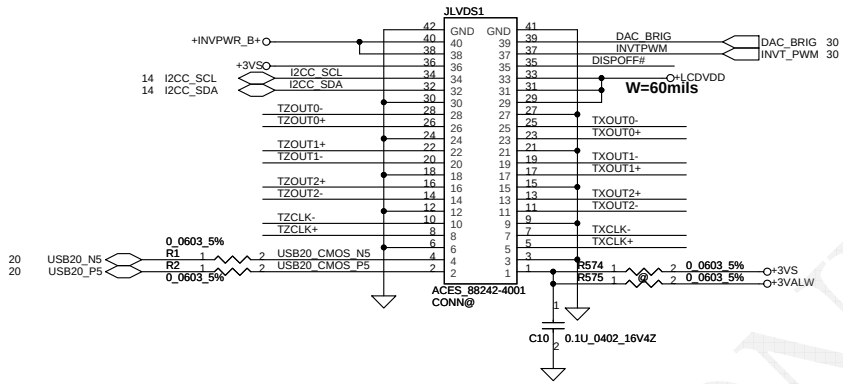
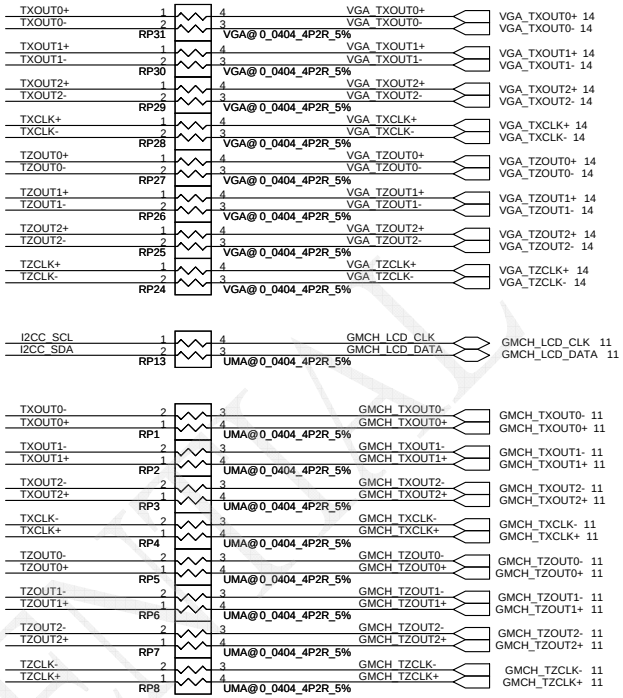
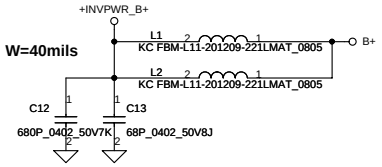
LCD POWER CIRCUIT

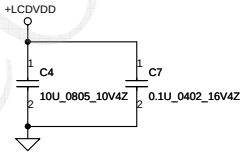


LCD/PANEL BD. Conn.









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reserve HDMI I2C ESD diode

DDC to Docking

38 EC_DOCKIN — EC_DOCKIN

11 GMCH_DDC_CLK — R89 LMA@ 0_0402_5%

14 VGA_DVI_SCLK — R88 VGA@ 0_0402_5% — VGA_DVI_SCLK_R

14 VGA_DVI_SDATA — R98 VGA@ 0_0402_5% — VGA_DVI_SDATA_R

11 GMCH_DDC_DATA — R94 LMA@ 0_0402_5%

+HDMI_5V_OUT

R90 2K_0402_5% — R91 2K_0402_5%

BSH111 1N_SOT23-3 Q48 — D_DVI_SCLK 38

BSH111 1N_SOT23-3 Q47 — D_DVI_SDATA 38

DDC to HDMI CONN

18,33,38 EC_DOCKIN#_S0 — EC_DOCKIN#_S0

+HDMI_5V_OUT

R84 6.8K_0402_5% — R87 6.8K_0402_5%

VGA_DVI_SCLK_R — HDMI_SCLK

VGA_DVI_SDATA_R — HDMI_SDATA

BSH111 1N_SOT23-3 Q50

BSH111 1N_SOT23-3 Q49

Place closed to JHDMI1

JHDMI1 — TYCO_1939864-1 — CONN@

Pin	Signal
19	HDMI_HPD
18	+5V (+HDMI_5V_OUT)
17	DDC/CEC_GND
16	HDMI_SDATA — SDA
15	HDMI_SCLK — SCL
14	Reserved
13	CEC
12	HDMI_R_CK- — CK-
11	CK_shield
10	HDMI_R_CK+ — CK+
9	HDMI_R_D0+ — D0-
8	D0_shield
7	HDMI_R_D0+ — D0+
6	HDMI_R_D1- — D1-
5	D1_shield
4	HDMI_R_D1+ — D1+
3	HDMI_R_D2- — D2-
2	D2_shield
1	HDMI_R_D2+ — D2+
20, 21, 22, 23	GND

U41 — SN74CBTD3306CPWR_TSSOP8 @

Pin	Signal
1A	VGA_DVI_SCLK_R
2A	VGA_DVI_SDATA_R
1OE#	EC_DOCKIN#_S0
2OE#	GND
VCC	+HDMI_5V_OUT
1B	D_DVI_SCLK
2B	D_DVI_SDATA

U42 — SN74CBTD3306CPWR_TSSOP8 @

Pin	Signal
1A	VGA_DVI_SCLK_R
2A	VGA_DVI_SDATA_R
1OE#	EC_DOCKIN
2OE#	GND
VCC	+HDMI_5V_OUT
1B	HDMI_SCLK
2B	HDMI_SDATA

+5VS — D6 RB491D_SC59-3 — F1 1.1A_6VDC_FUSE — +HDMI_5V_OUT

W=40mils

C177 0.1U_0402_16V4Z

R524 0_0402_5% — D_DVI_DET 38

+HDMI_5V_OUT — C243 0.1U_0402_16V7K

R123 2.2K_0402_5% — +3VS

U9 SN74AHCT1G125GW_SOT353-5 — HDMI_DET 11,14

R105 100K_0402_5% — C242 0.1U_0402_16V7K

HDMI_HPD

HDMI_CLK- — R382 0_0402_5% — HDMI_R_CK-

L50 @WCM-2012-900T_0805

HDMI_CLK+ — R383 0_0402_5% — HDMI_R_CK+

HDMI_TX0- — R384 0_0402_5% — HDMI_R_D0-

L51 @WCM-2012-900T_0805

HDMI_TX0+ — R385 0_0402_5% — HDMI_R_D0+

HDMI_TX1- — R386 0_0402_5% — HDMI_R_D1-

L52 @WCM-2012-900T_0805

HDMI_TX1+ — R387 0_0402_5% — HDMI_R_D1+

HDMI_TX2- — R388 0_0402_5% — HDMI_R_D2-

L53 @WCM-2012-900T_0805

HDMI_TX2+ — R390 0_0402_5% — HDMI_R_D2+

+3VS — R393 4.7K_0402_5% — MS

R392 @ 0_0402_5%

+3VS — D22 RB751V_SOD323 — OE

R400 4.7K_0402_5%

+3VS — D21 SS1040_SOD123

+3VS_D80

C486 0.1U_0402_16V4Z — C485 0.1U_0402_16V4Z

NOTE: L : D-->A
H: D-->B

U28 — PI3HDMI412ADZBE_TQFN56_8X8

Pin	Signal
4	14 VGA_DVI_TXC+ — D0+
5	14 VGA_DVI_TXC- — D0-
7	14 VGA_DVI_TXD0+ — D1+
8	14 VGA_DVI_TXD0- — D1-
9	14 VGA_DVI_TXD1+ — D2+
10	14 VGA_DVI_TXD1- — D2-
12	14 VGA_DVI_TXD2+ — D3+
13	14 VGA_DVI_TXD2- — D3-
16	T12 PAD — SEL_OUT
55	T13 PAD @ — SEL_IN
19	8,9,15,20,28 ICH_SMBCLK0 @ — SCL/S3
20	8,9,15,20,28 ICH_SMBDATA0 — SDA/S2
1	MS — MS
17	T11 PAD — TEST_OUT
54	@ — TEST_IN
56	OE — OE
49	A0 — A0/S4
50	A1 — A1/S5
51	A2 — A2/S6
52	A3 — A3/S7
25	HDMI_TX2- — D3-_B
26	HDMI_TX2+ — D3+_B
28	HDMI_TX1- — D2-_B
29	HDMI_TX1+ — D2+_B
31	HDMI_TX0- — D1-_B
32	HDMI_TX0+ — D1+_B
34	HDMI_CLK- — D0-_B
35	HDMI_CLK+ — D0+_B
37	D_DVI_TXD2- 38 — D3-_A
38	D_DVI_TXD2+ 38 — D3+_A
40	D_DVI_TXD1- 38 — D2-_A
41	D_DVI_TXD1+ 38 — D2+_A
43	D_DVI_TXD0- 38 — D1-_A
44	D_DVI_TXD0+ 38 — D1+_A
46	D_DVI_TXC- 38 — D0-_A
47	D_DVI_TXC+ 38 — D0+_A
18, 57	NC, T-pad
2, 6, 11, 15, 24, 36, 48, 22	VDD1, VDD2, VDD3, VDD4, VDD5, VDD6, VDD7, AVDD
3, 14, 21, 27, 30, 33, 39, 42, 45, 53, 23	VSS1, VSS2, VSS3, VSS4, VSS5, VSS6, VSS7, VSS8, VSS9, VSS10, AVSS

+3VS — R395 @4.7K_0402_5% — R401 0_0402_5% — A0

+3VS — R396 @4.7K_0402_5% — R402 0_0402_5% — A1

+3VS — R397 @4.7K_0402_5% — R403 0_0402_5% — A2

+3VS — R398 @4.7K_0402_5% — R404 0_0402_5% — A3

SMBus Address: 1100 000X (b)

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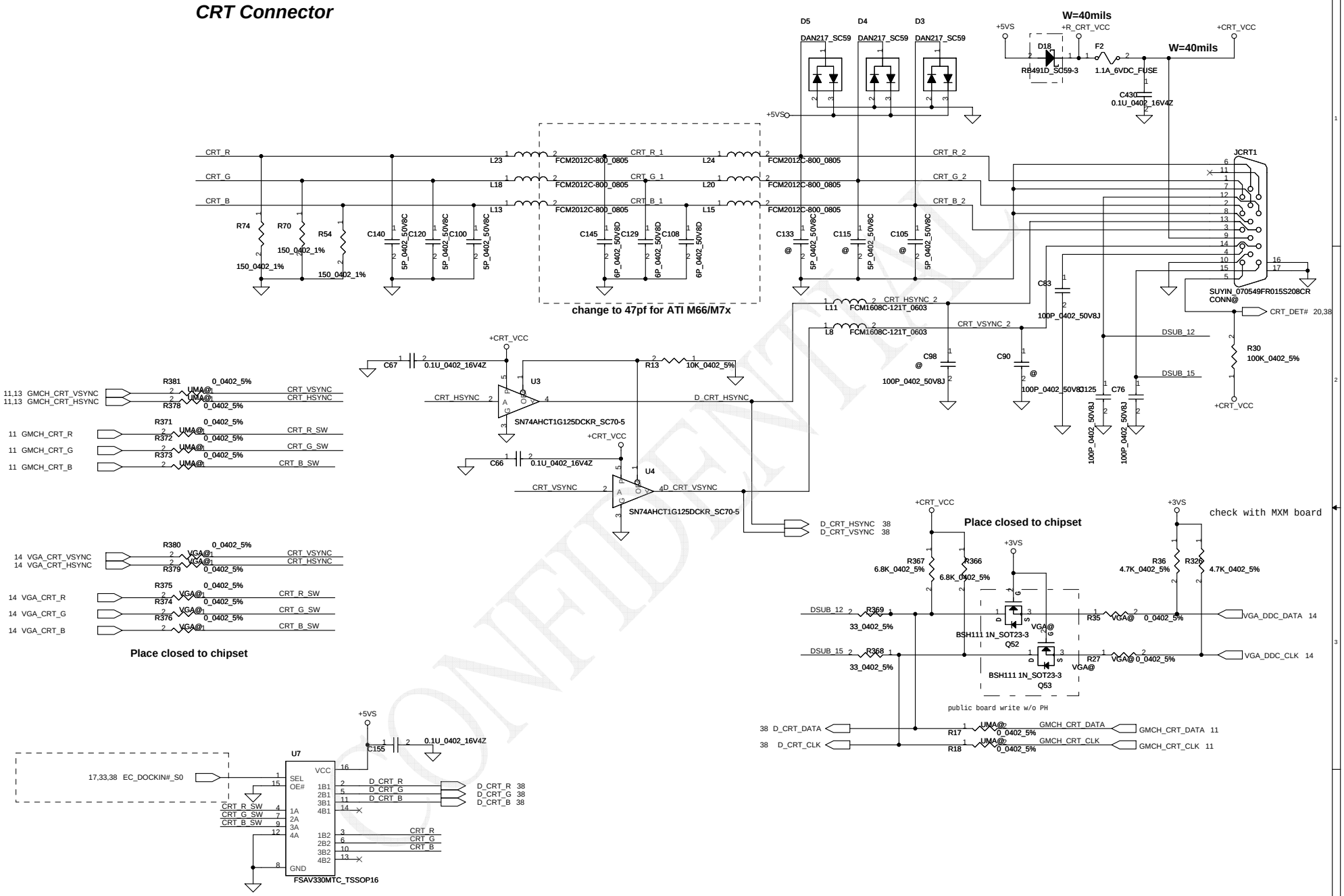
CRT Connector



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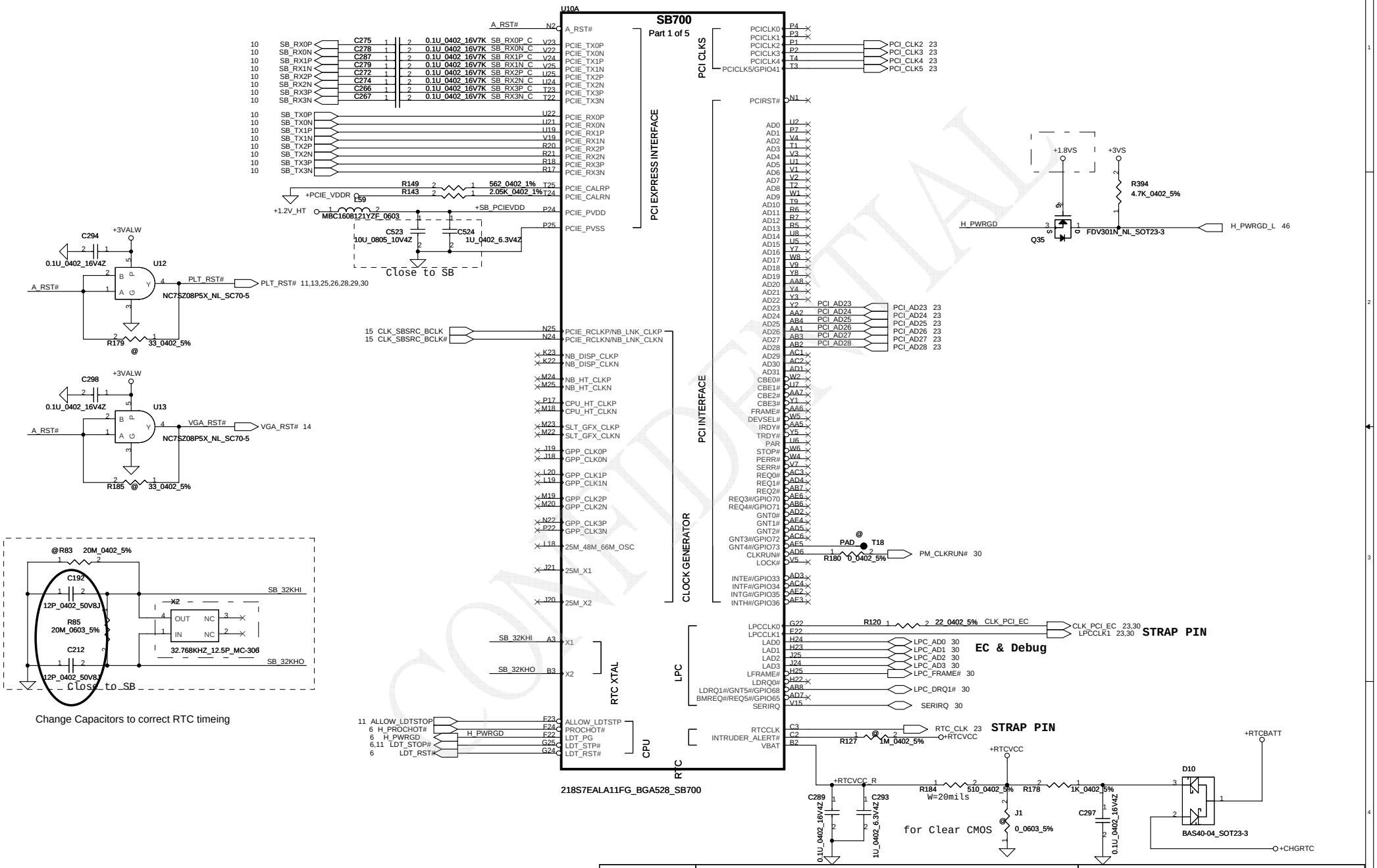

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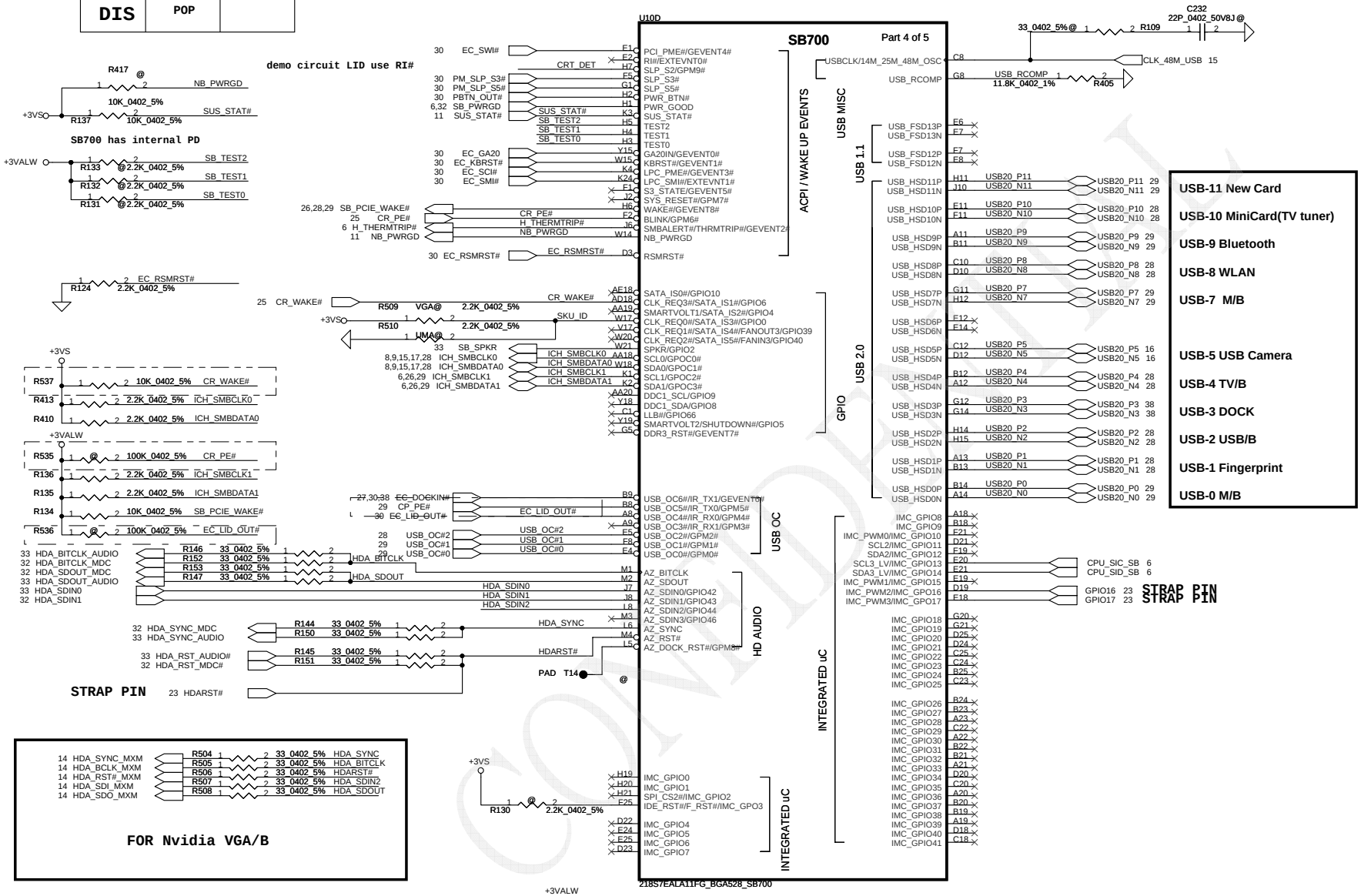
SKU-ID	R509	R510
UMA		POP
DIS	POP	

demo circuit LID use RI#

SB700 has internal PD



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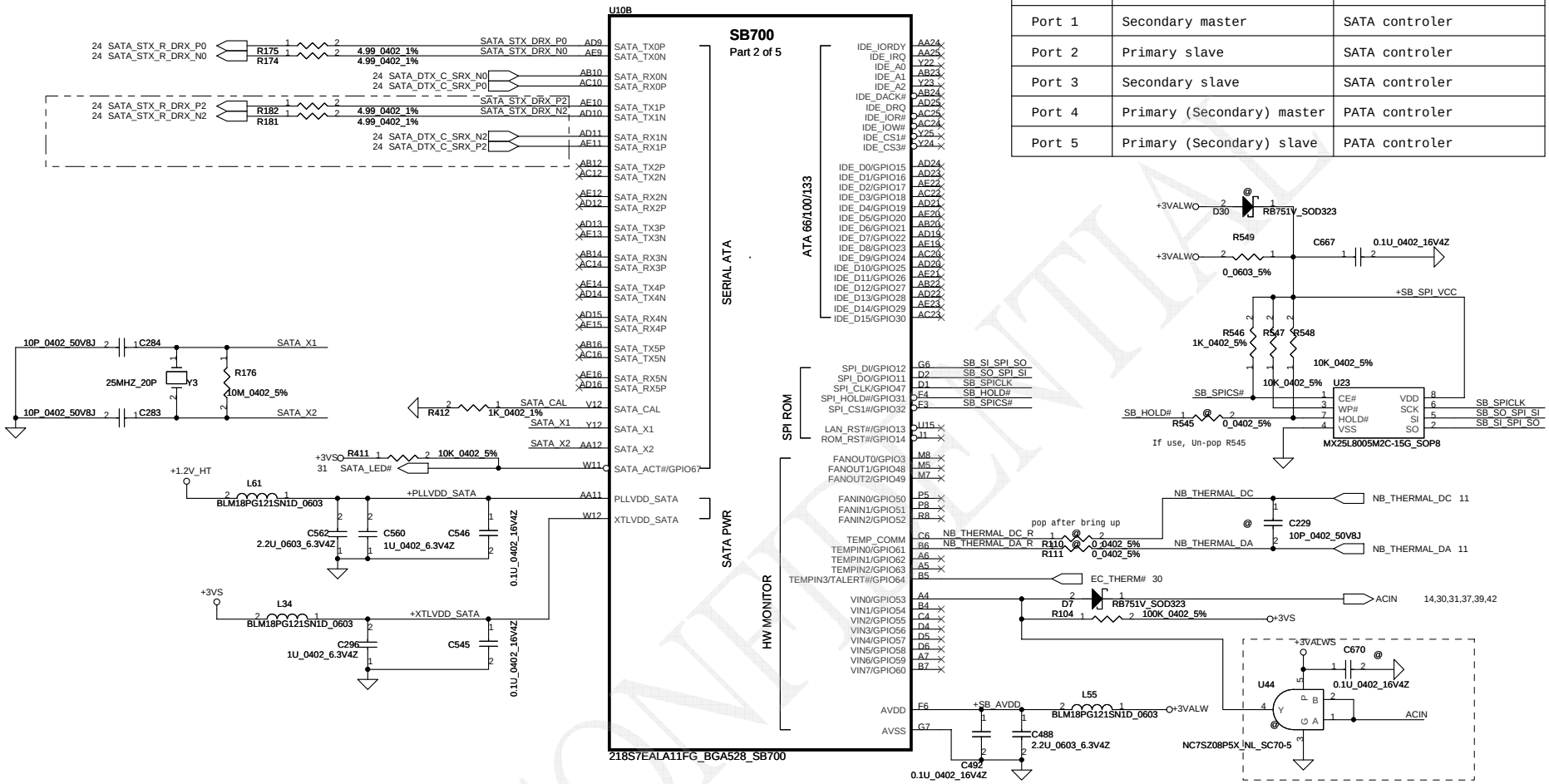
Port Number	Pri/SEC,Mas/Slave assignment	SATA drive controlled by
Port 0	Primary master	SATA controler
Port 1	Secondary master	SATA controler
Port 2	Primary slave	SATA controler
Port 3	Secondary slave	SATA controler
Port 4	Primary (Secondary) master	PATA controler
Port 5	Primary (Secondary) slave	PATA controler



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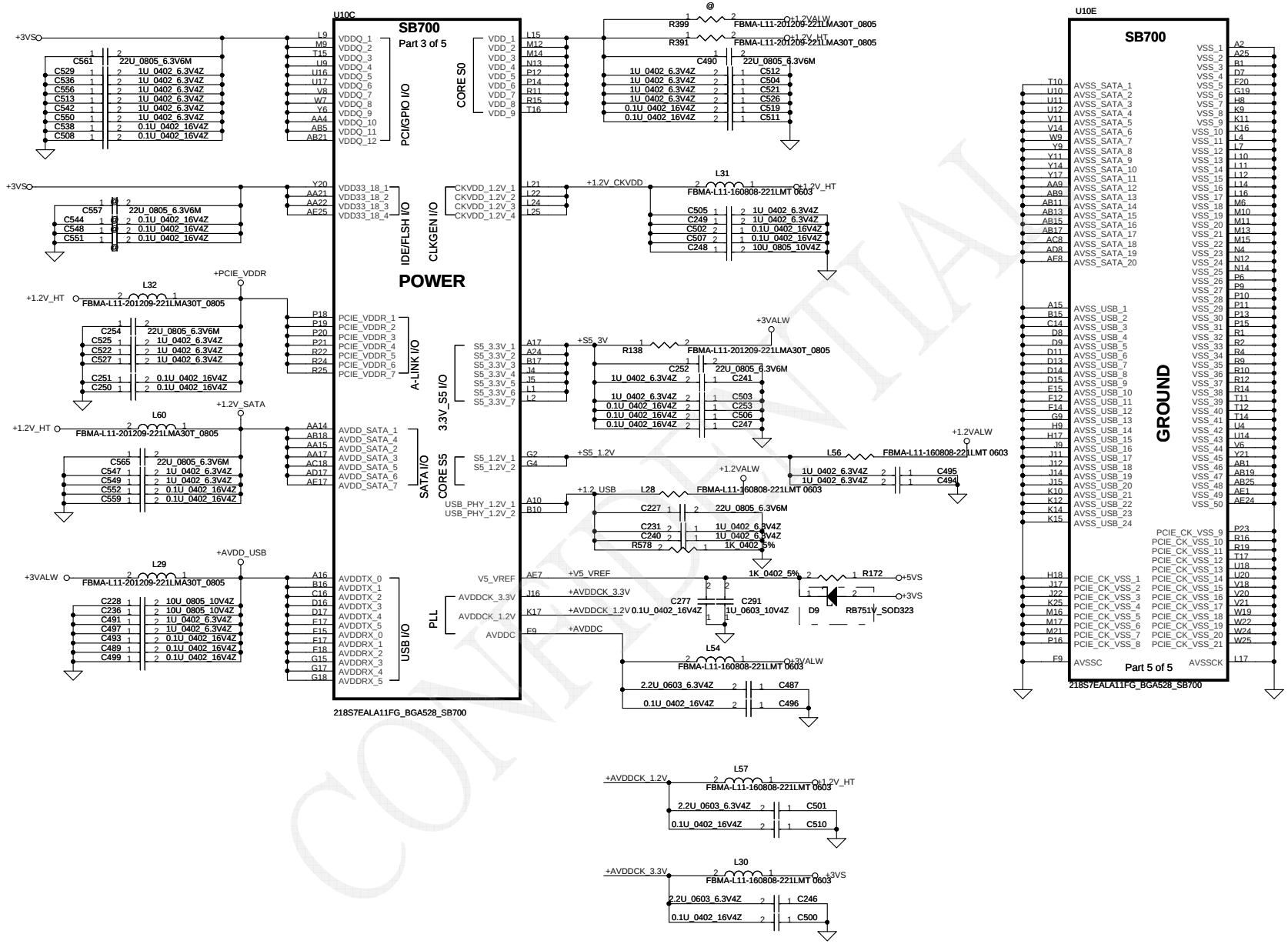
FOR SB700 ALL issue
A12 Will change to +1.2V_HT



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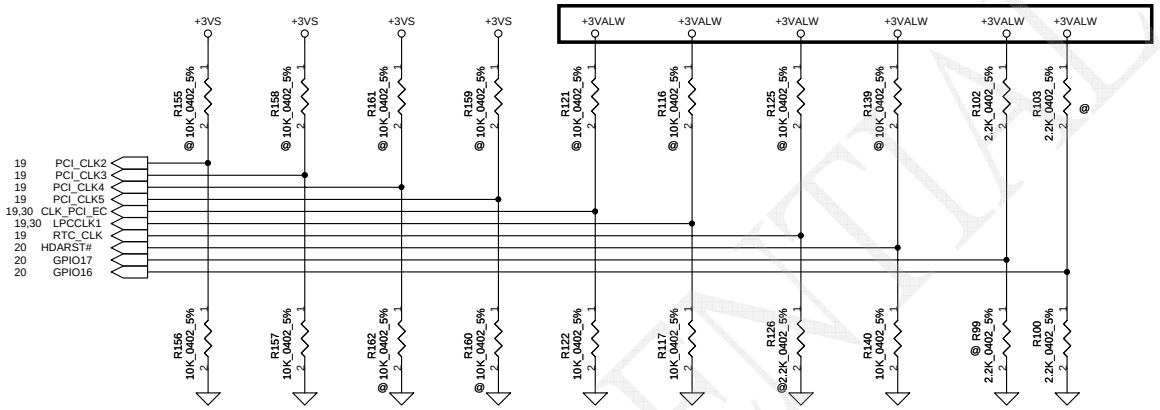
REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

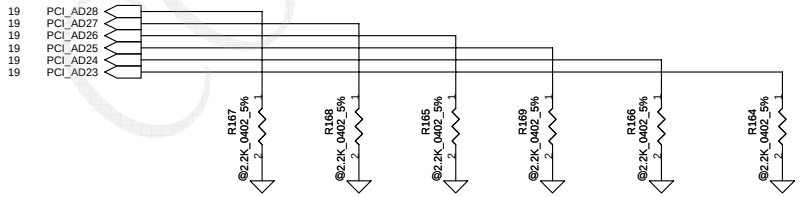
	PCI_CLK2 CLK_PCI_PCM	PCI_CLK3 CLK_PCI_DBG	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	**INTERNAL RTC** DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM **L,H = LPC ROM (Default L,NC)** L,L = FWH ROM
PULL LOW	**BOOTFAIL TIMER DISABLED** DEFAULT	**IGNORE DEBUG STRAPS** DEFAULT			**DISABLE PCI MEM BOOT** DEFAULT	**CLKGEN DISABLED** DEFAULT	**EXT. RTC** (PD on X1, apply 32KHz to RTC_CLK)	**EC DISABLED** DEFAULT	



DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	**USE LONG RESET** DEFAULT	**USE PCI PLL** DEFAULT	**USE ACPI BCLK** DEFAULT	**USE IDE PLL** DEFAULT	**USE DEFAULT PCIE STRAPS** DEFAULT	**RESERVED**
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



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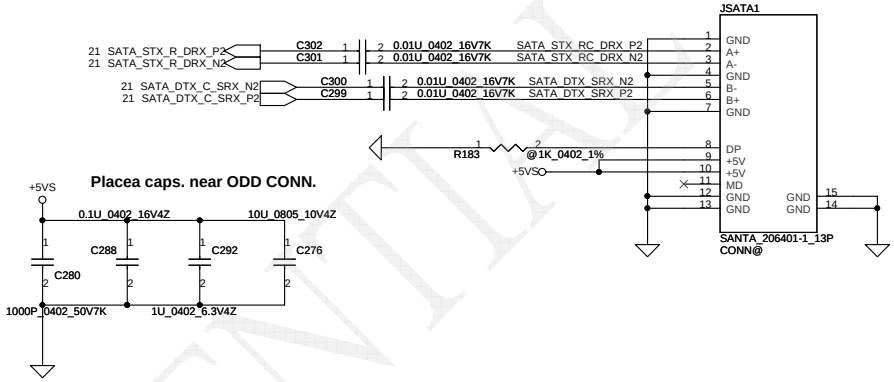
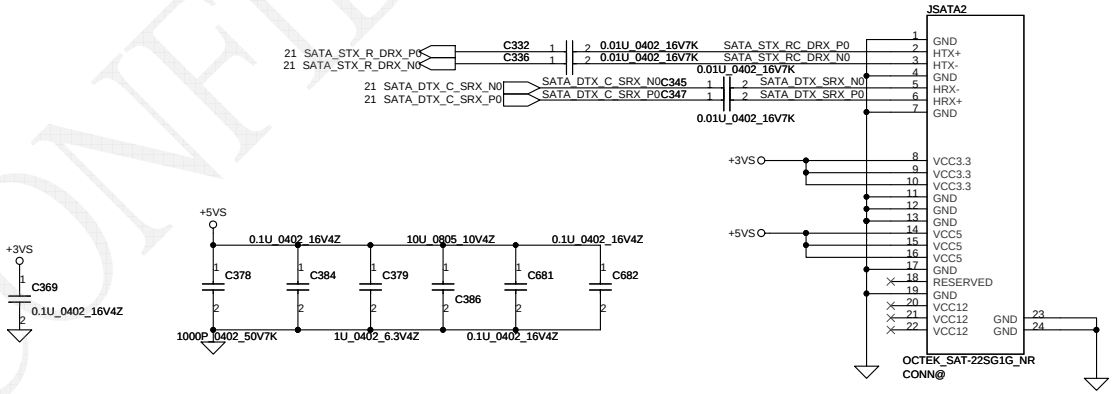
SATA ODD Conn.



SATA HDD Conn.



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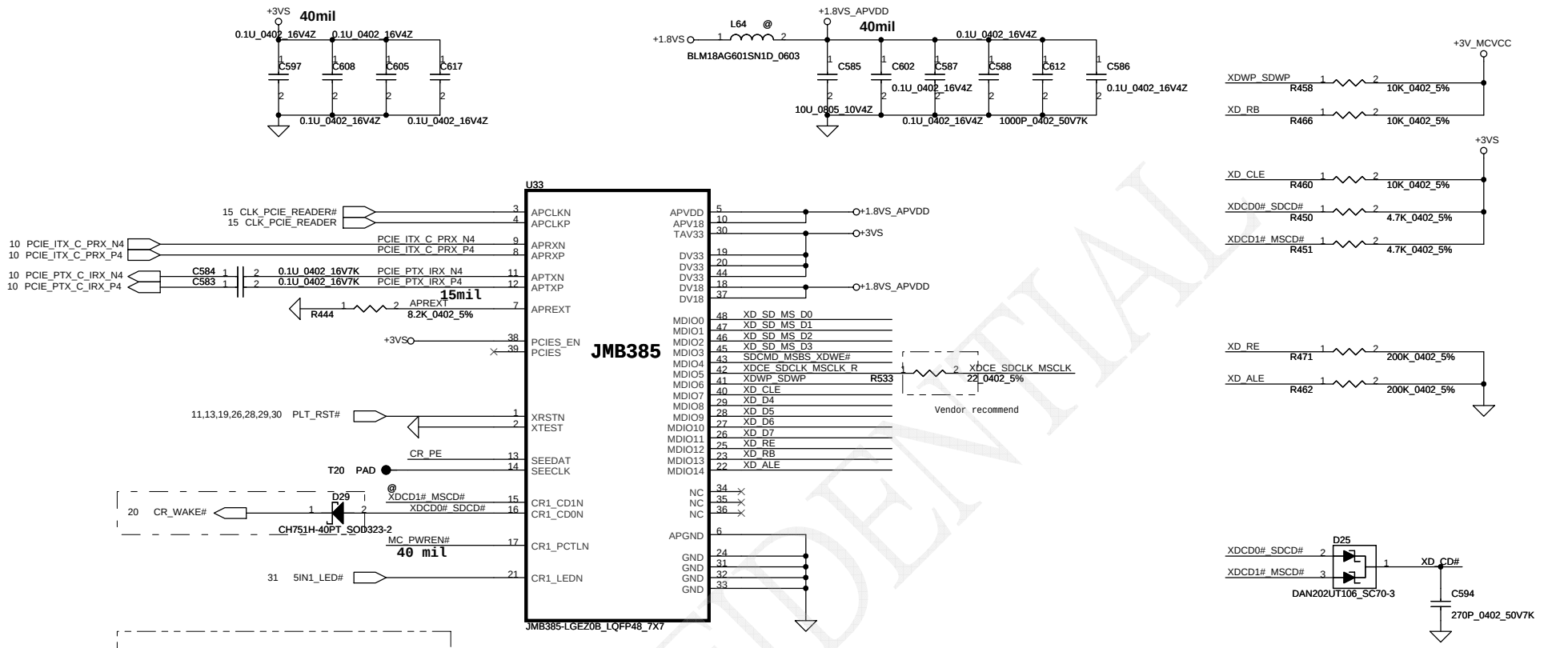
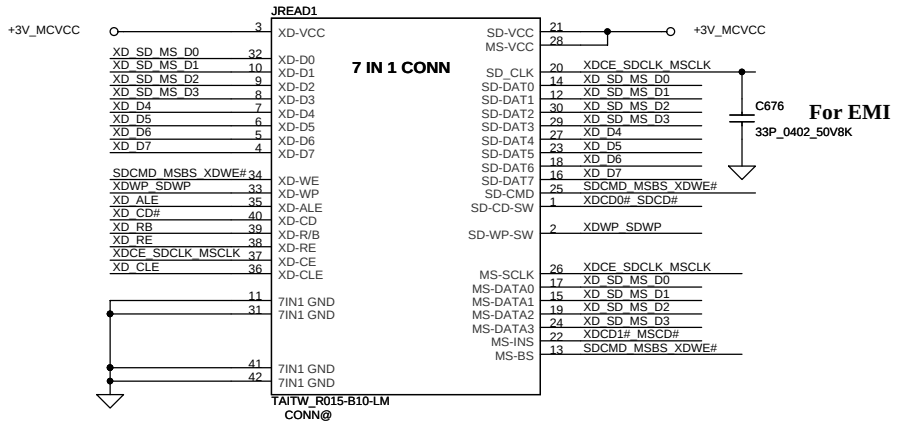


4 IN 1 Socket Push Type(New)



C620 must close Chipset

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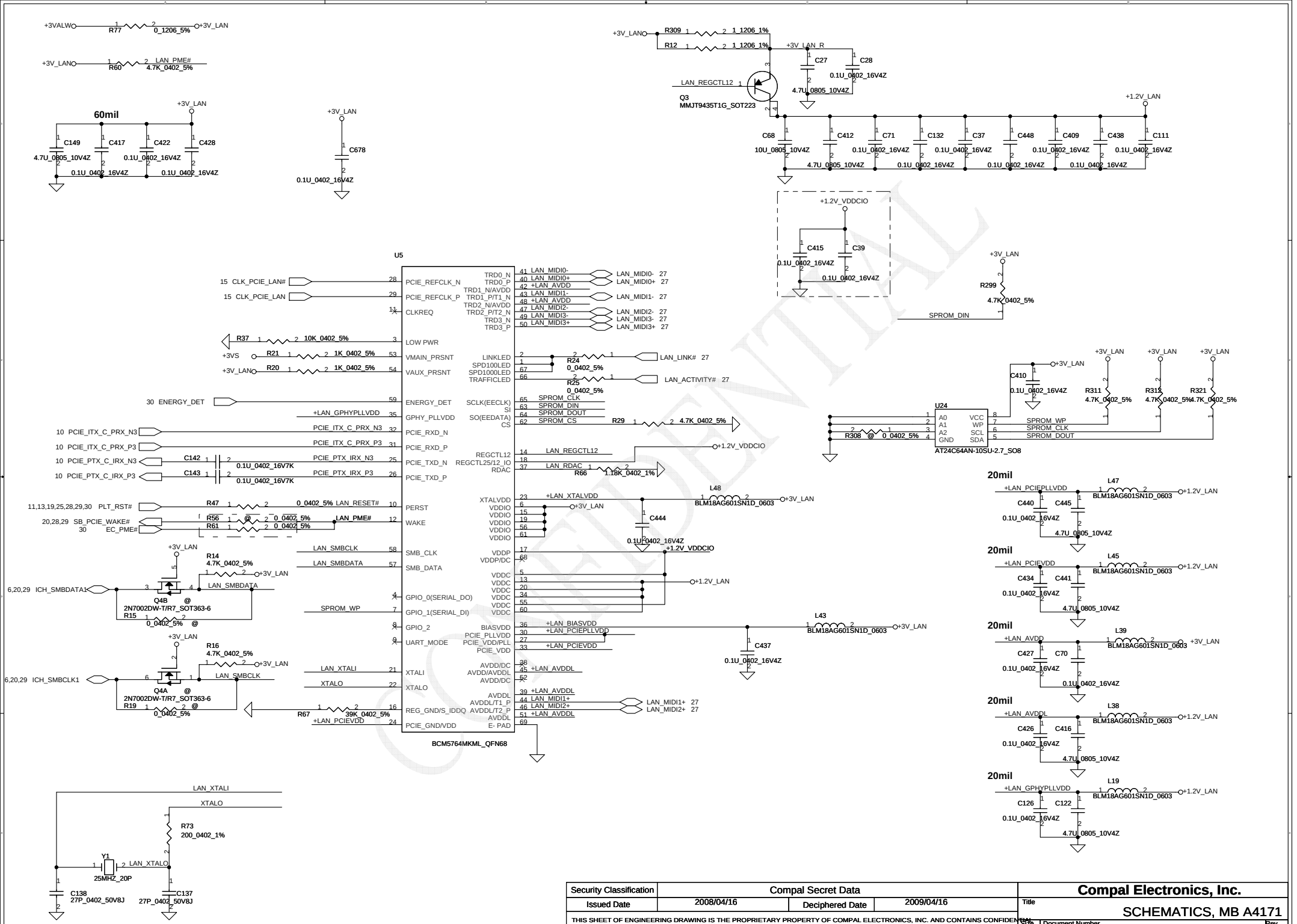

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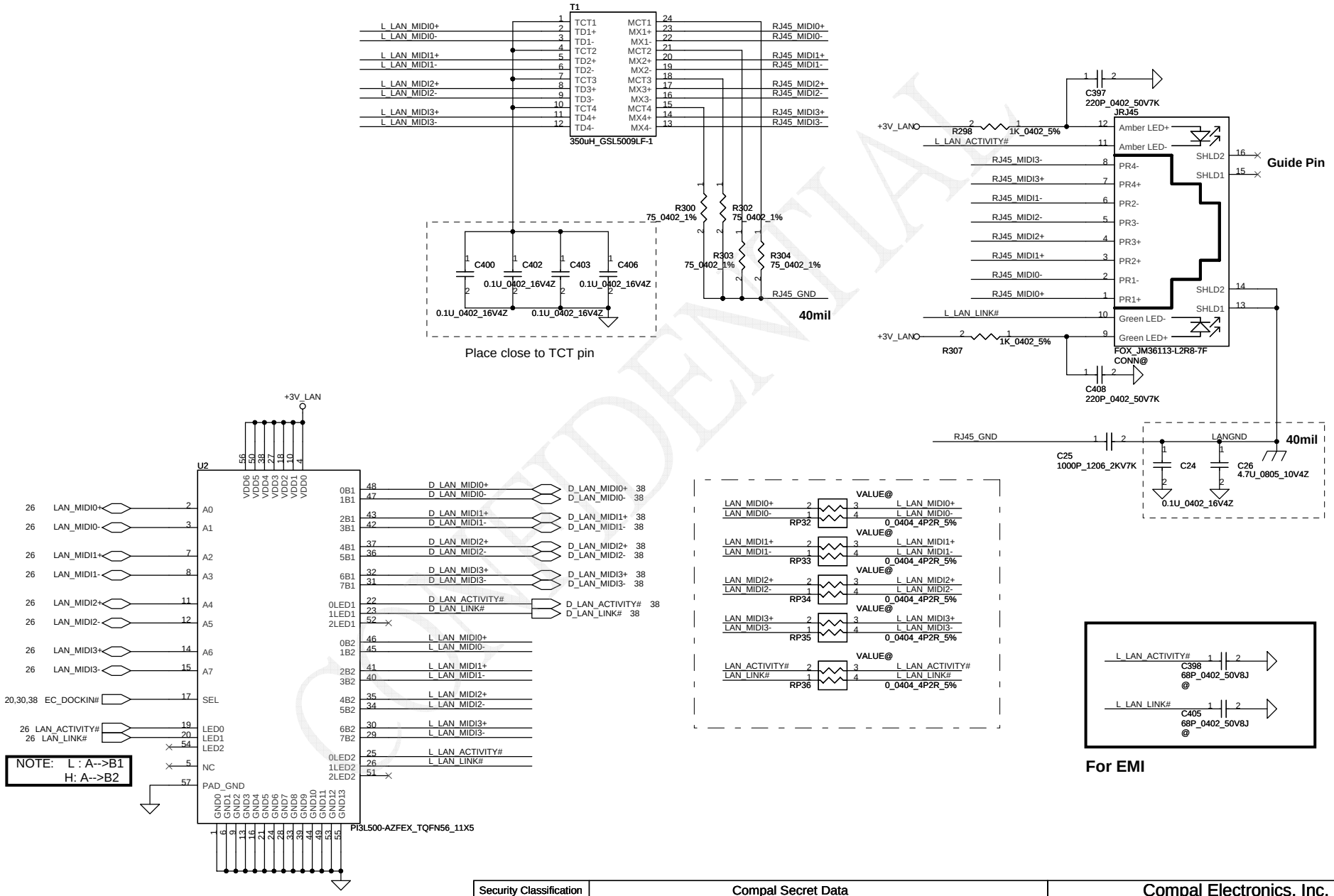

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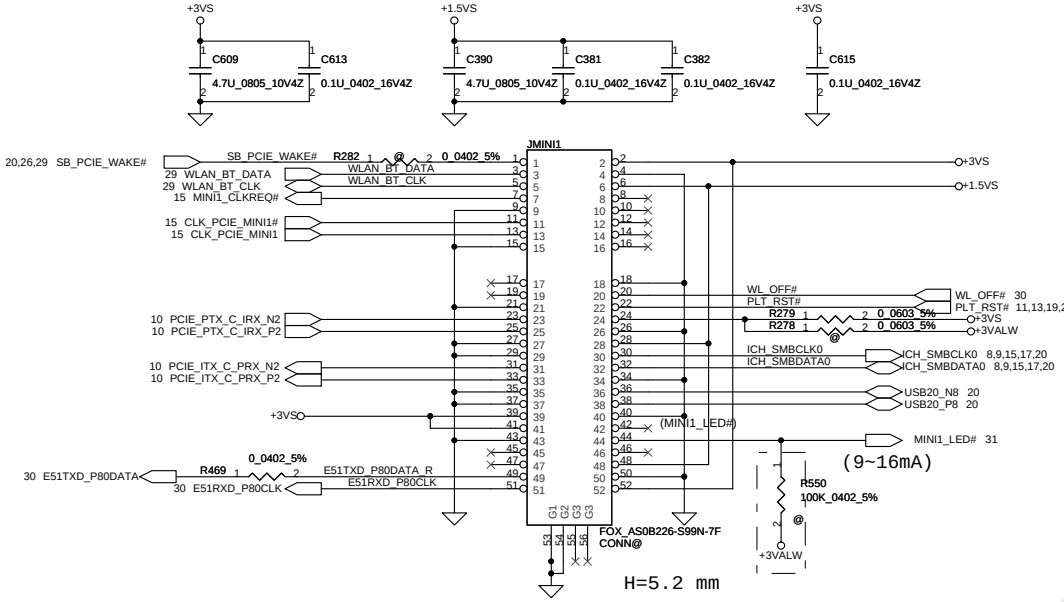
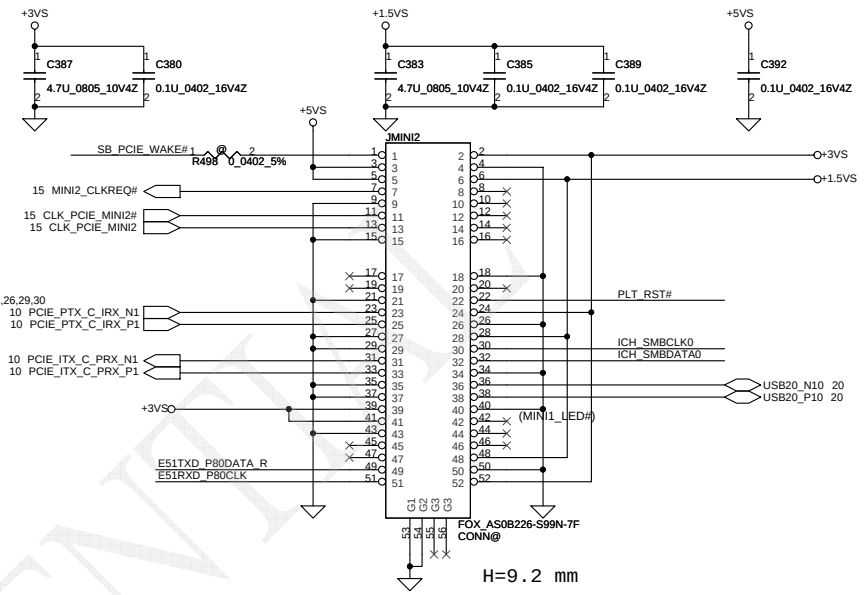
For Wireless LAN

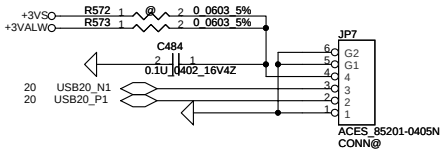


For TV-Tuner/HW MPEG

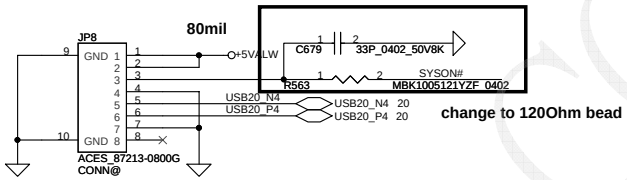


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

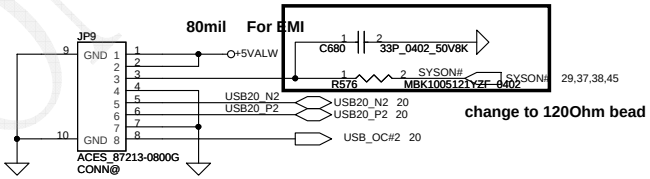
Fingerprint Conn

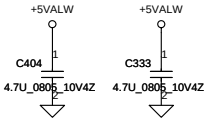


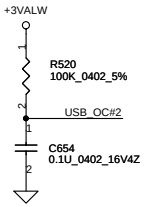
To USB/B Connector



To USB/B Connector







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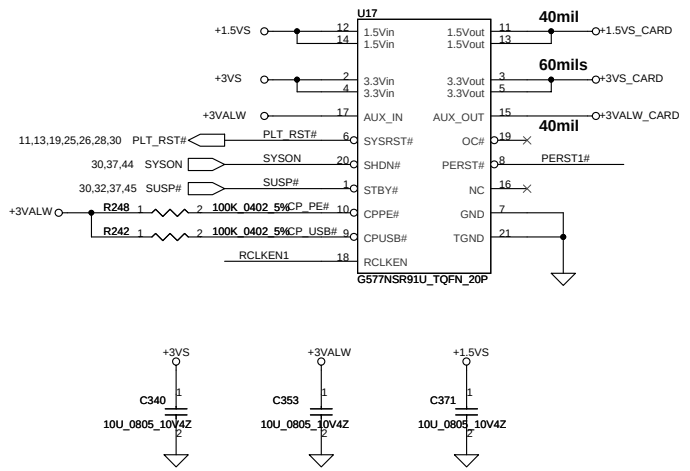
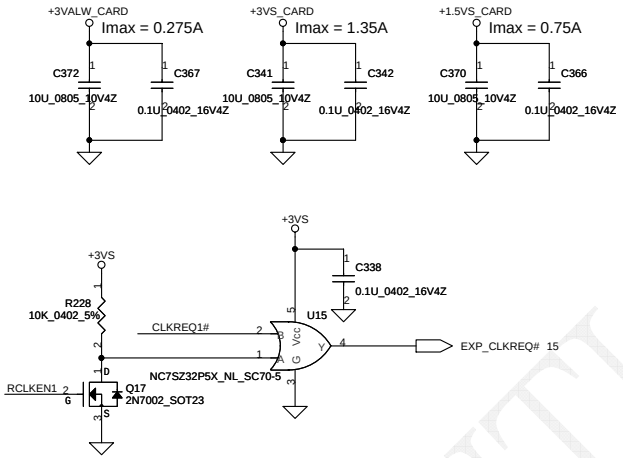
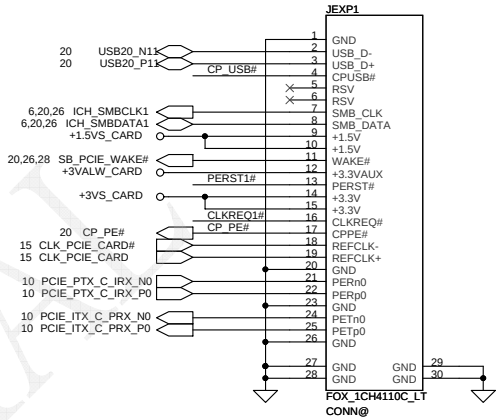
New Card Power Switch

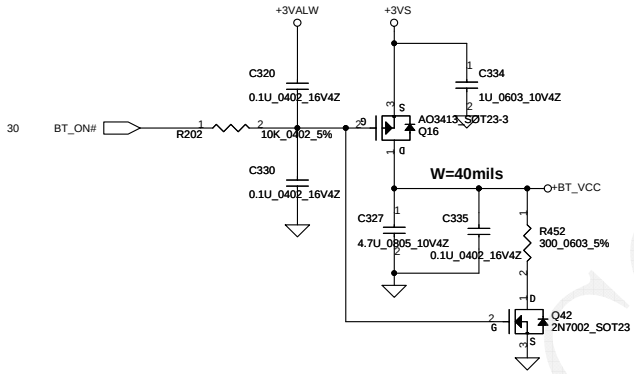


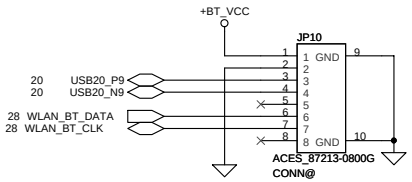


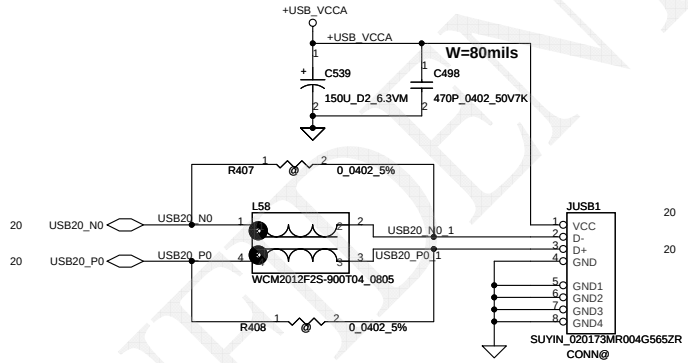
New Card Socket (Left/TOP)

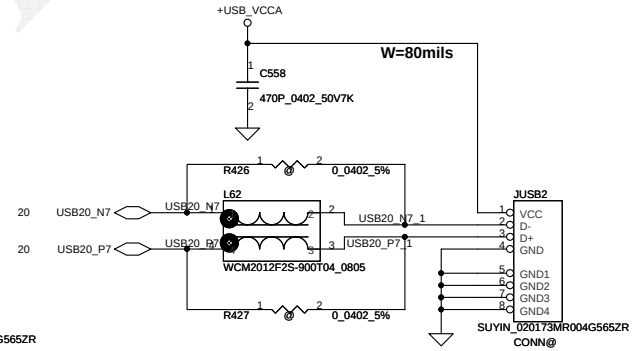


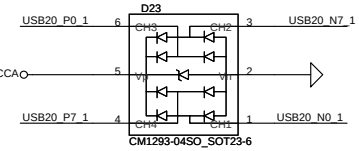
Bluetooth Conn.

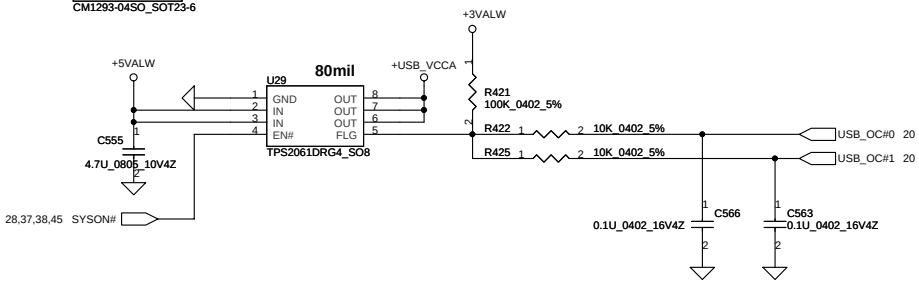












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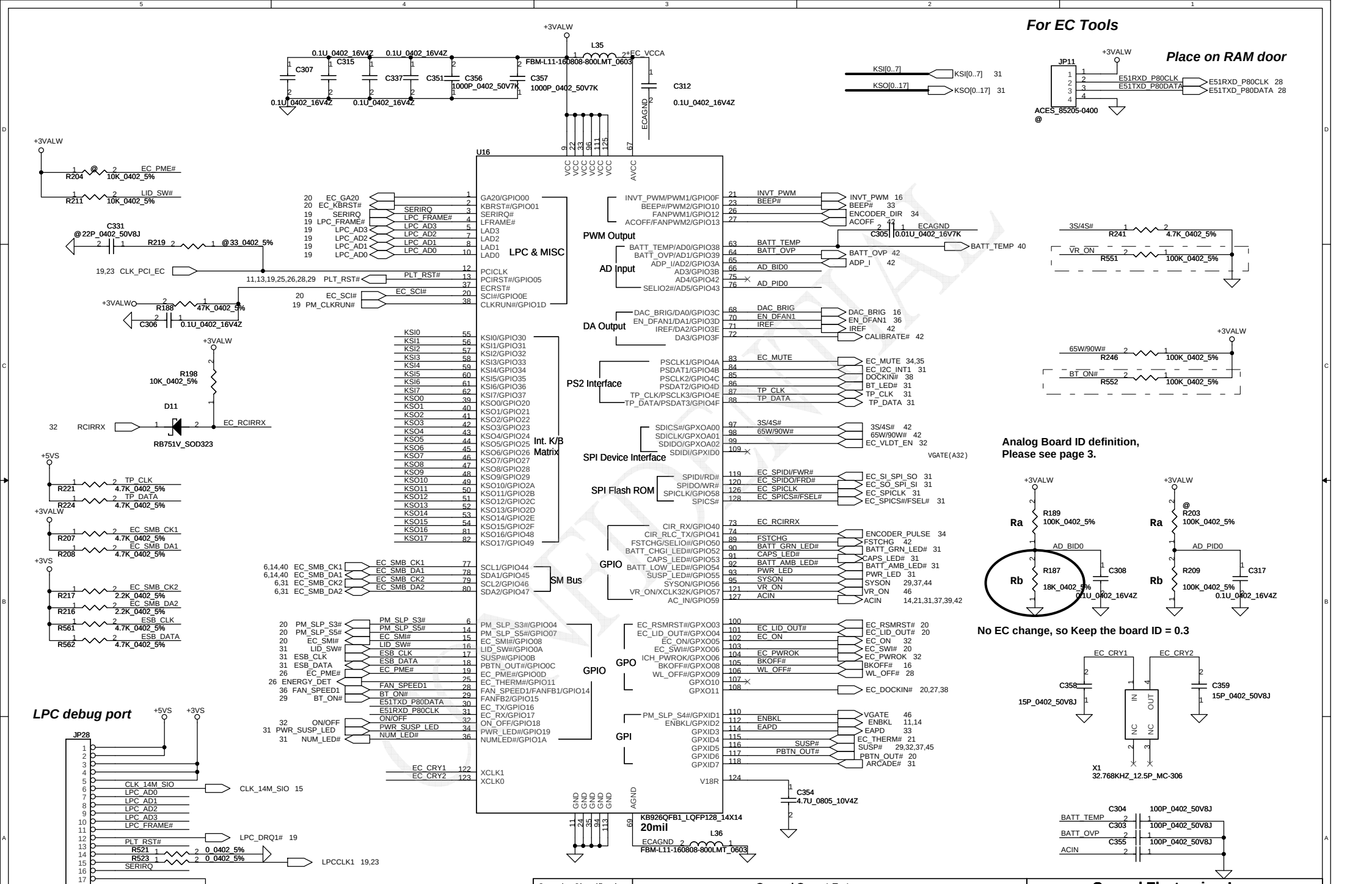
For EC Tools
Place on RAM door
JP11
ACES_85205-0400
U16
KB926QFB1_LQFP128_14X14
20mil
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
SM Bus
GPIO
GPO
GPI
Analog Board ID definition,
Please see page 3.
No EC change, so Keep the board ID = 0.3
LPC debug port
JP28
ACES_85201-20051
X1
32.768KHZ_12.5P_MC-306
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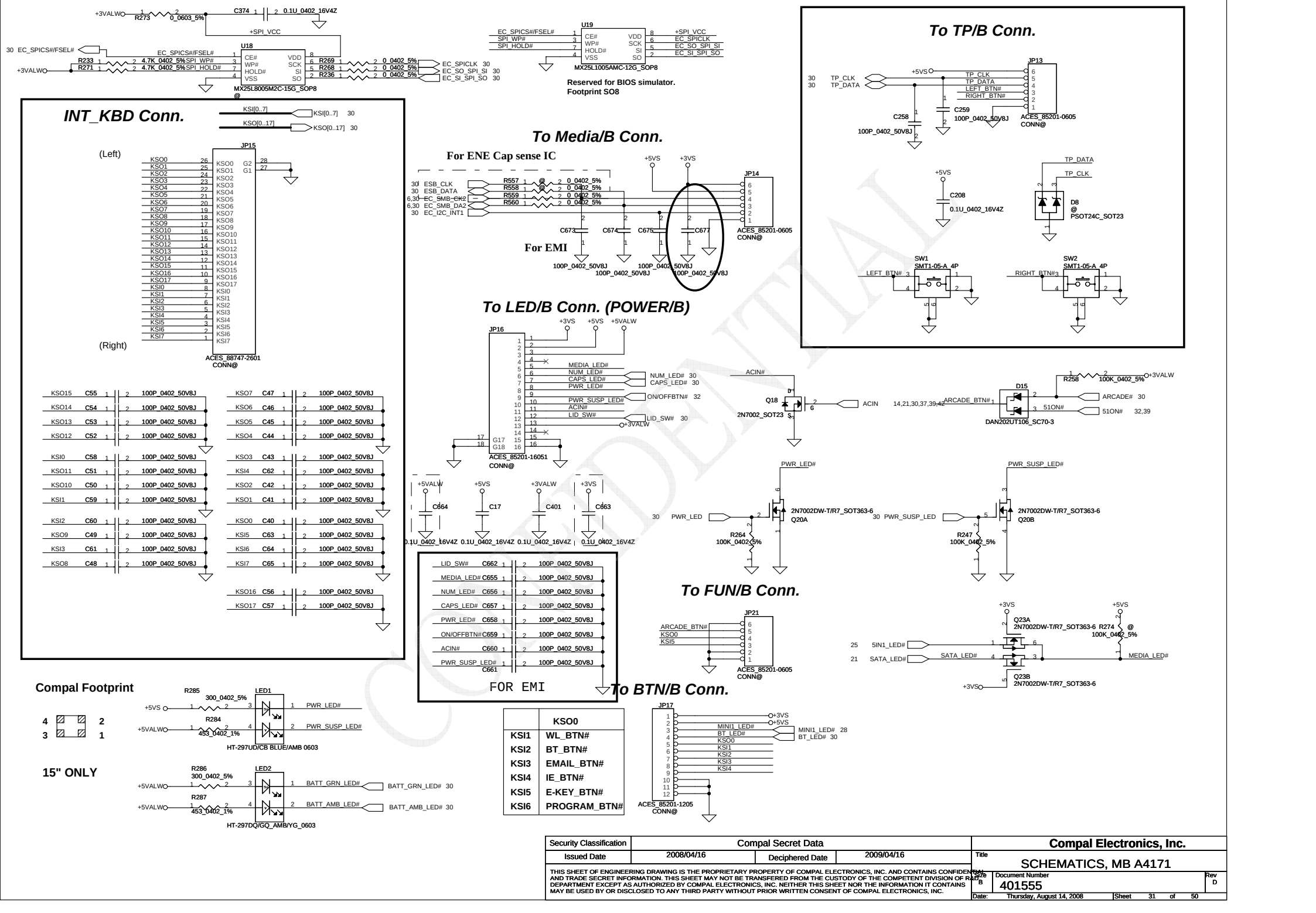

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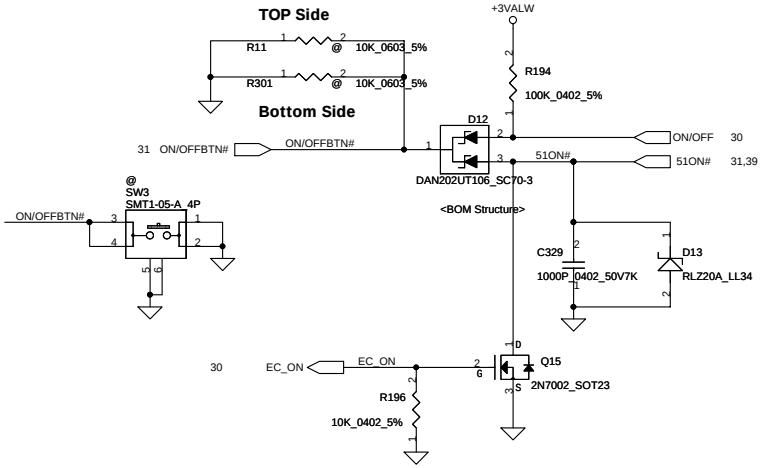
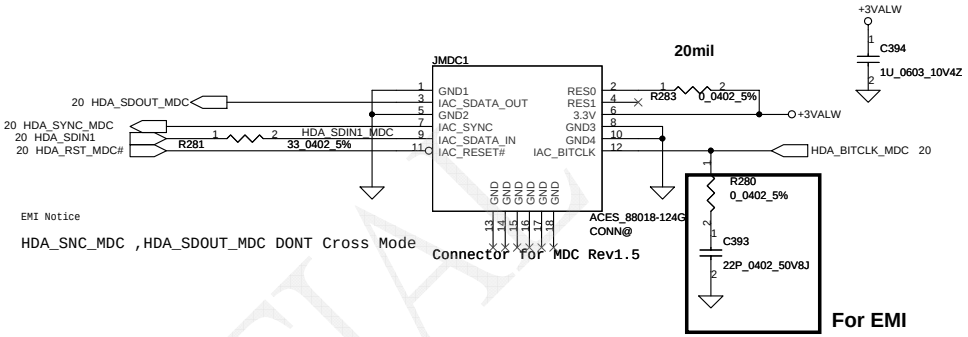
Power Button

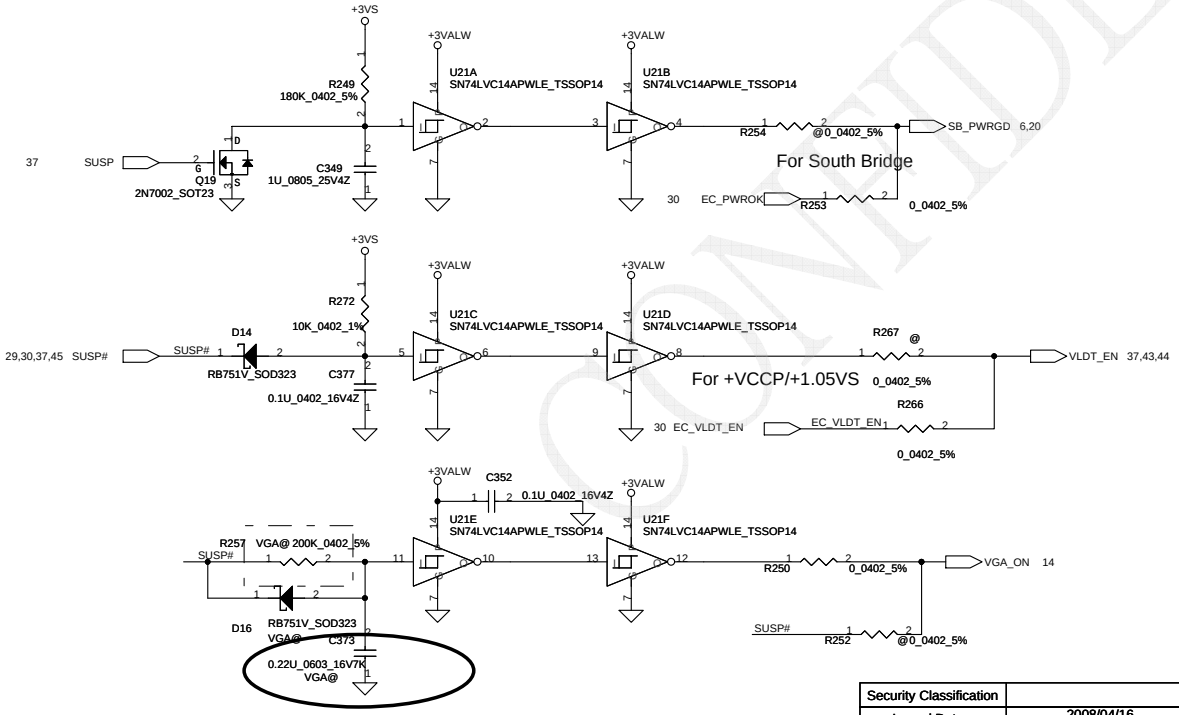
ON/OFF switch



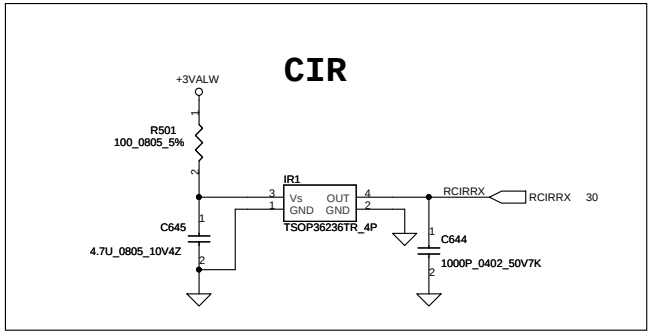
HDA MDC Conn.



Power ON Circuit



CIR



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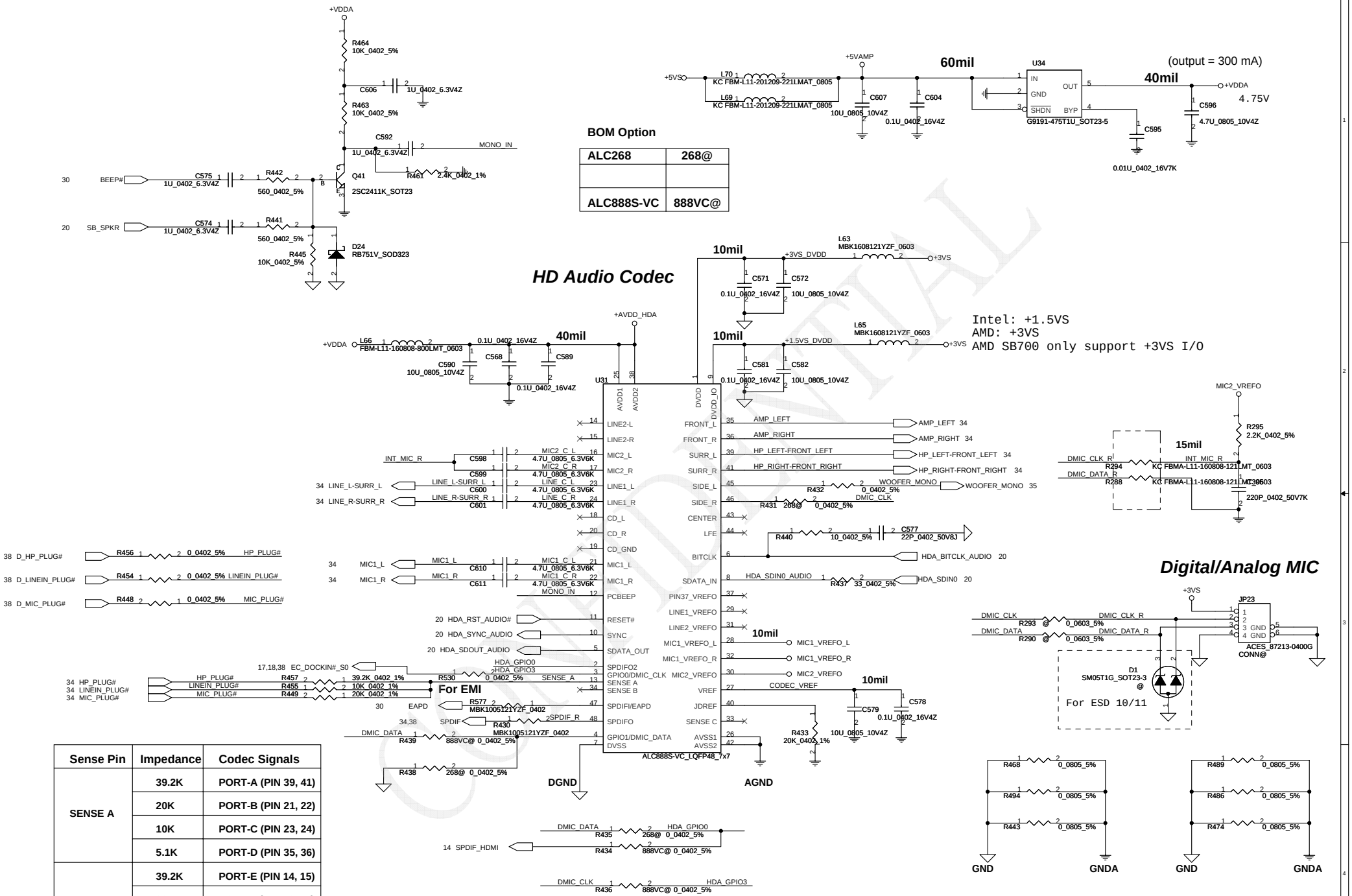
				Date: Thursday, August 14, 2008 / Sheet 32 of 50



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

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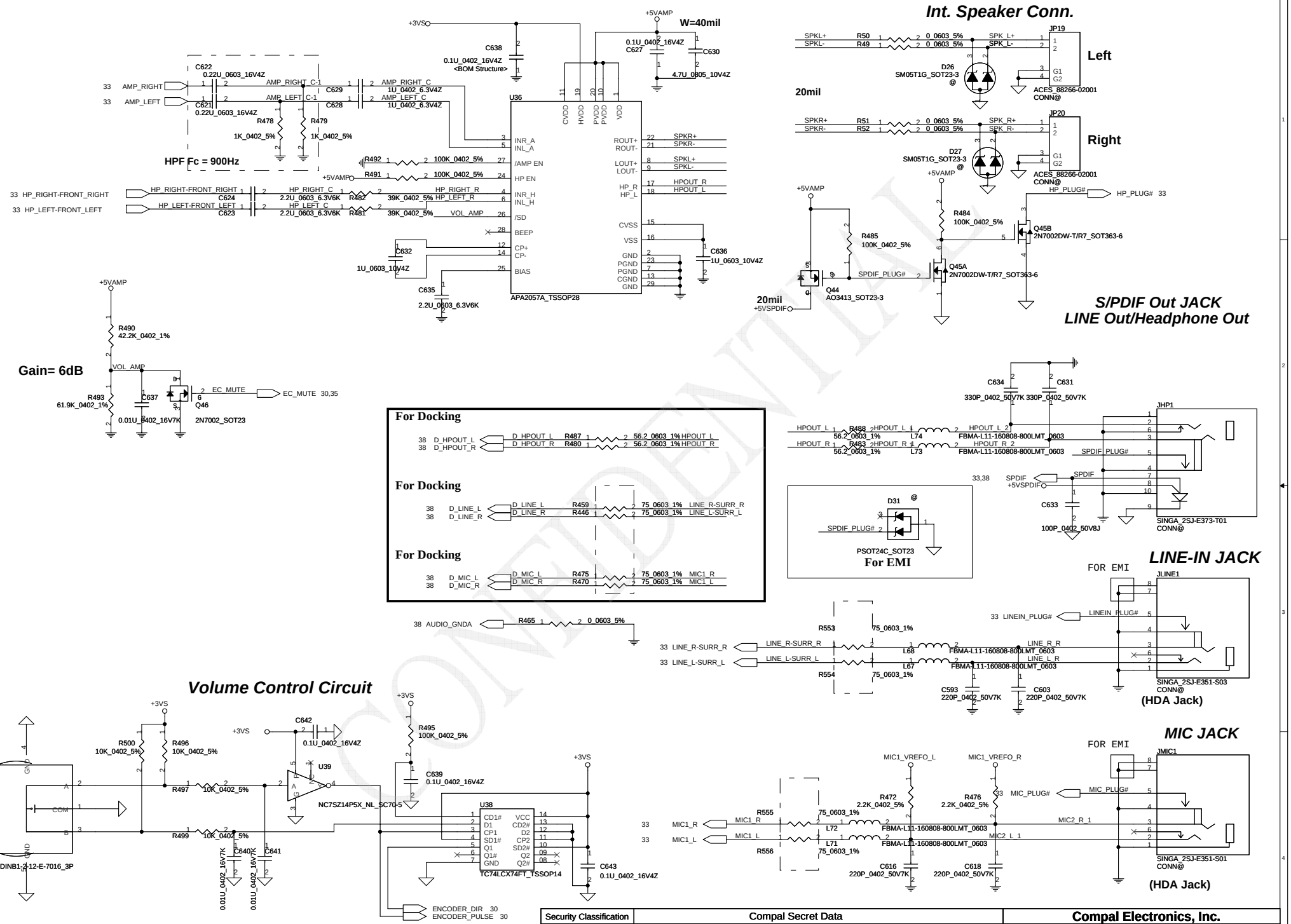

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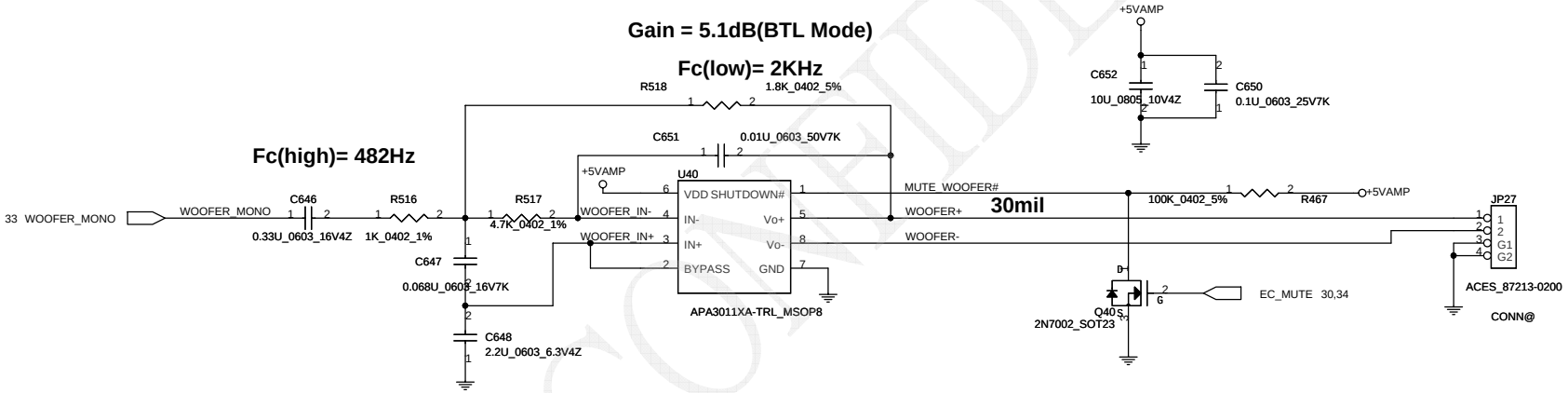
				Date: Thursday, August 14, 2008 / Sheet 34 of 50



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Title: **SCHEMATICS, MB A4171**

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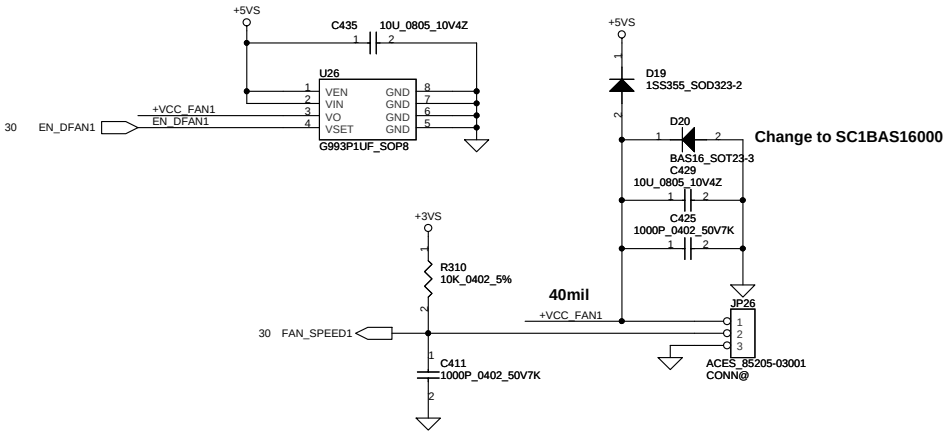
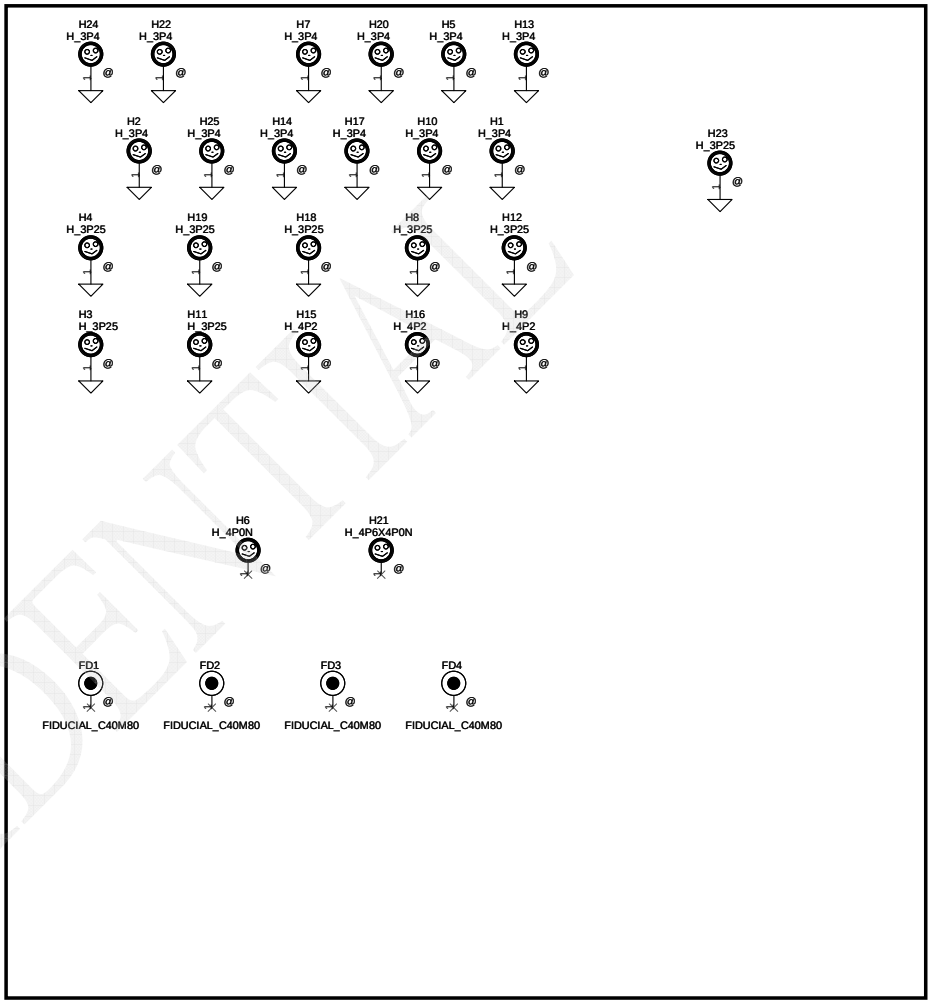
FAN1 Conn





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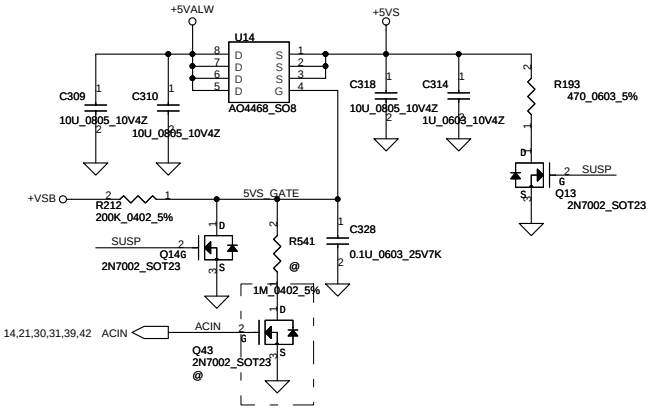
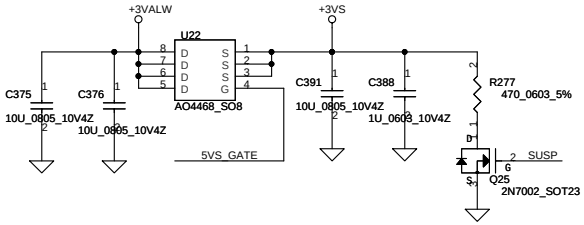
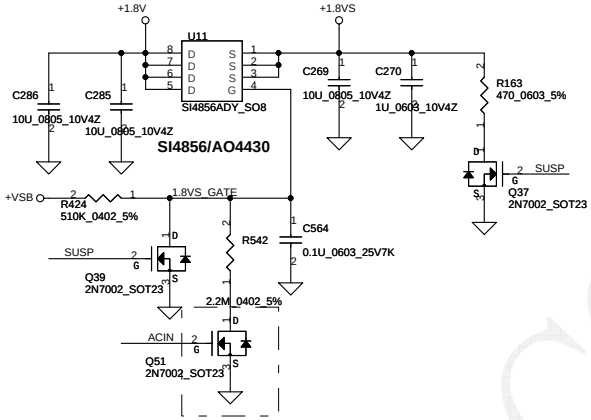
+5VALW TO +5VS

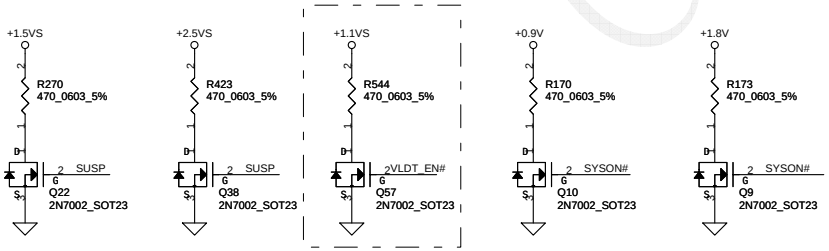


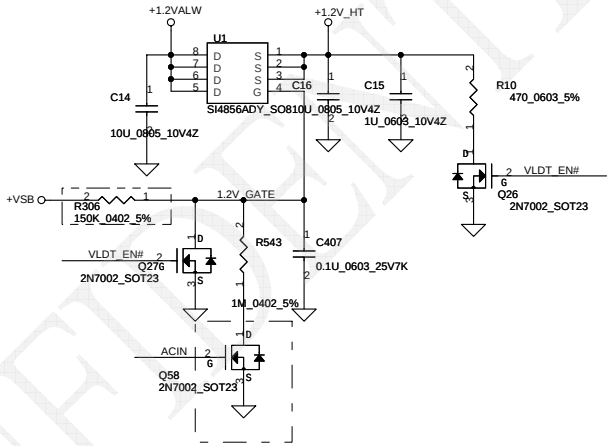
+3VALW TO +3VS

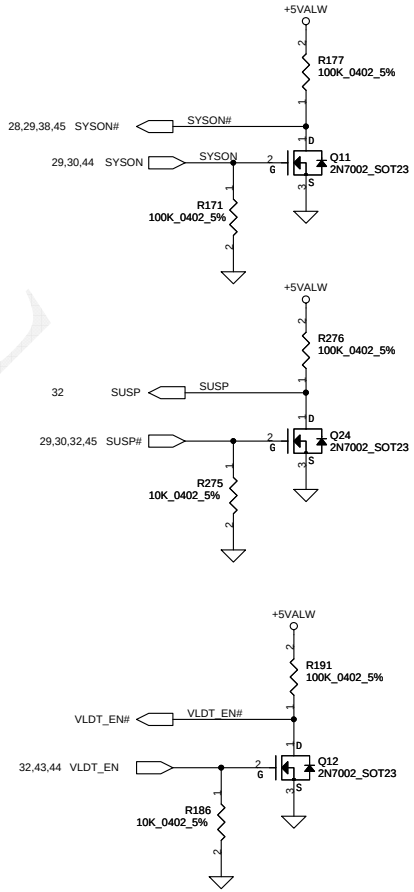


+1.8V to +1.8VS









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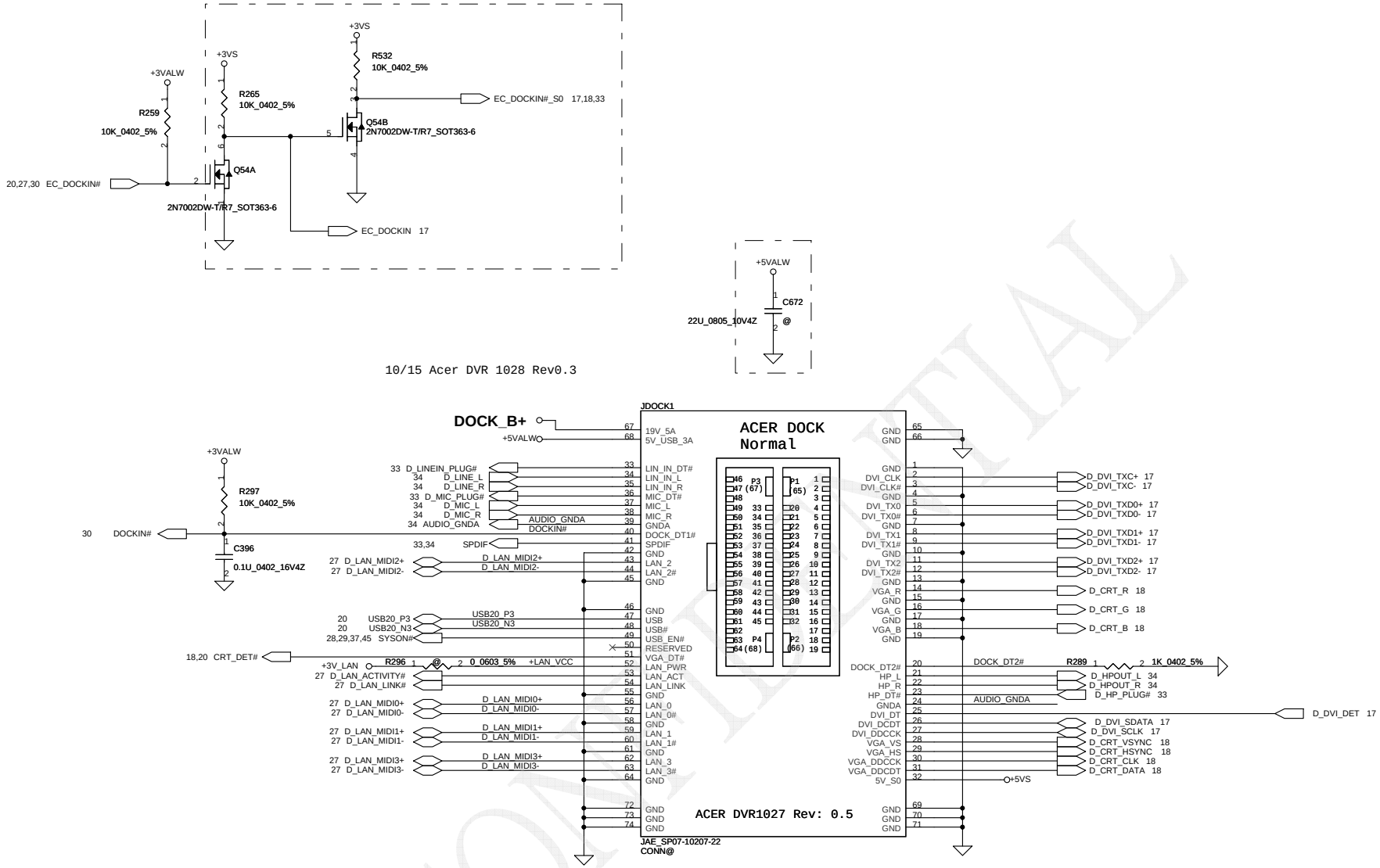

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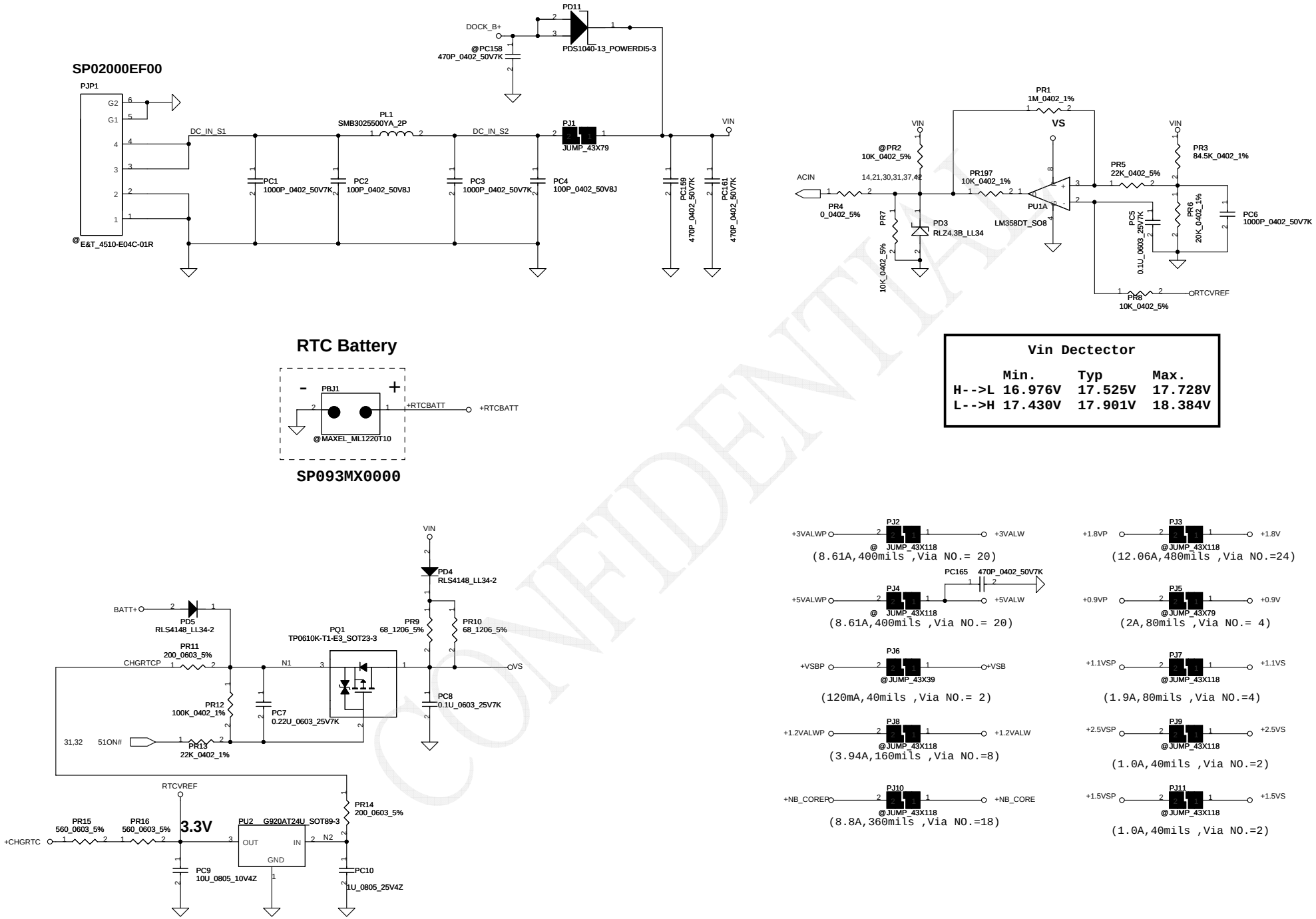

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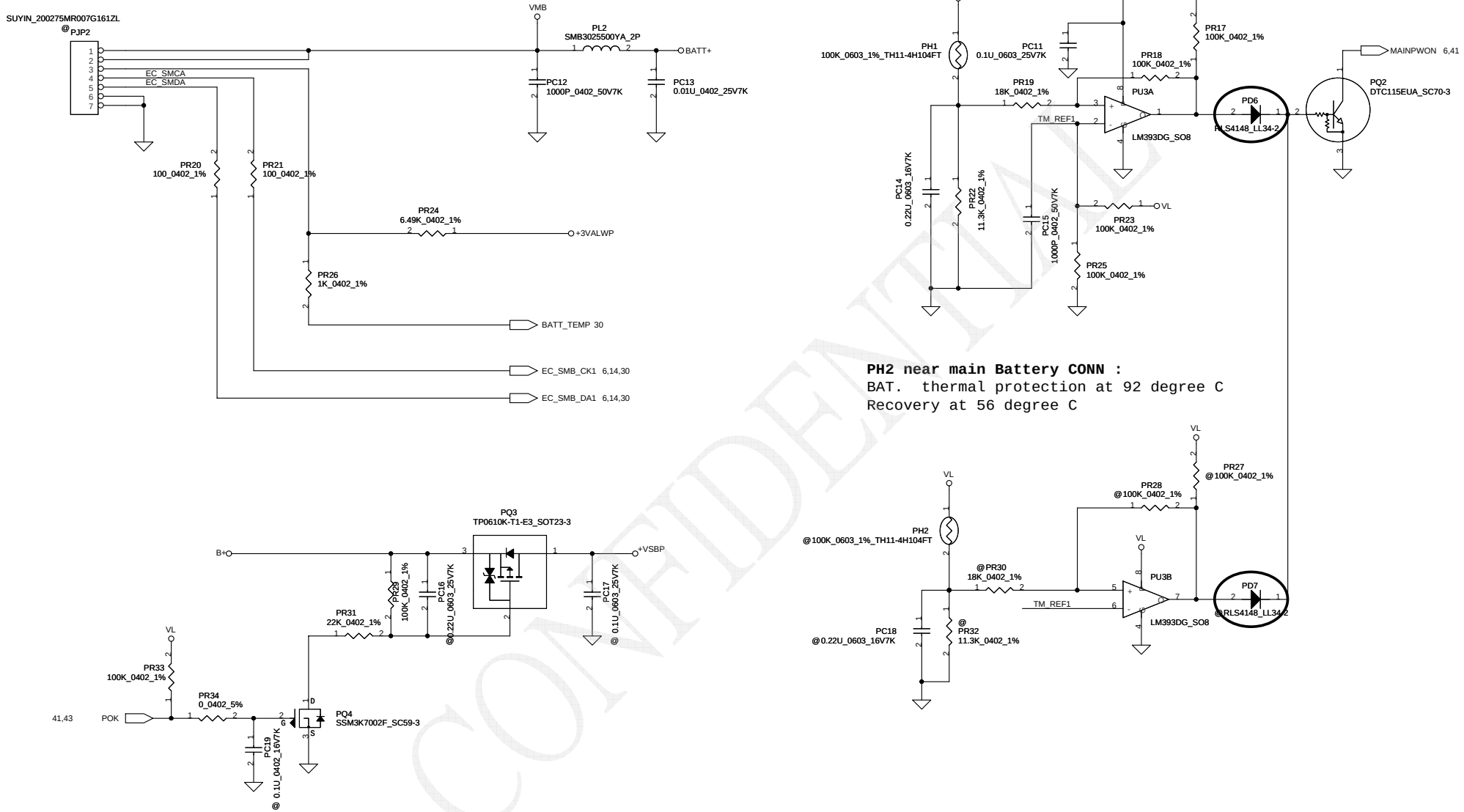
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 92 degree C
Recovery at 56 degree C

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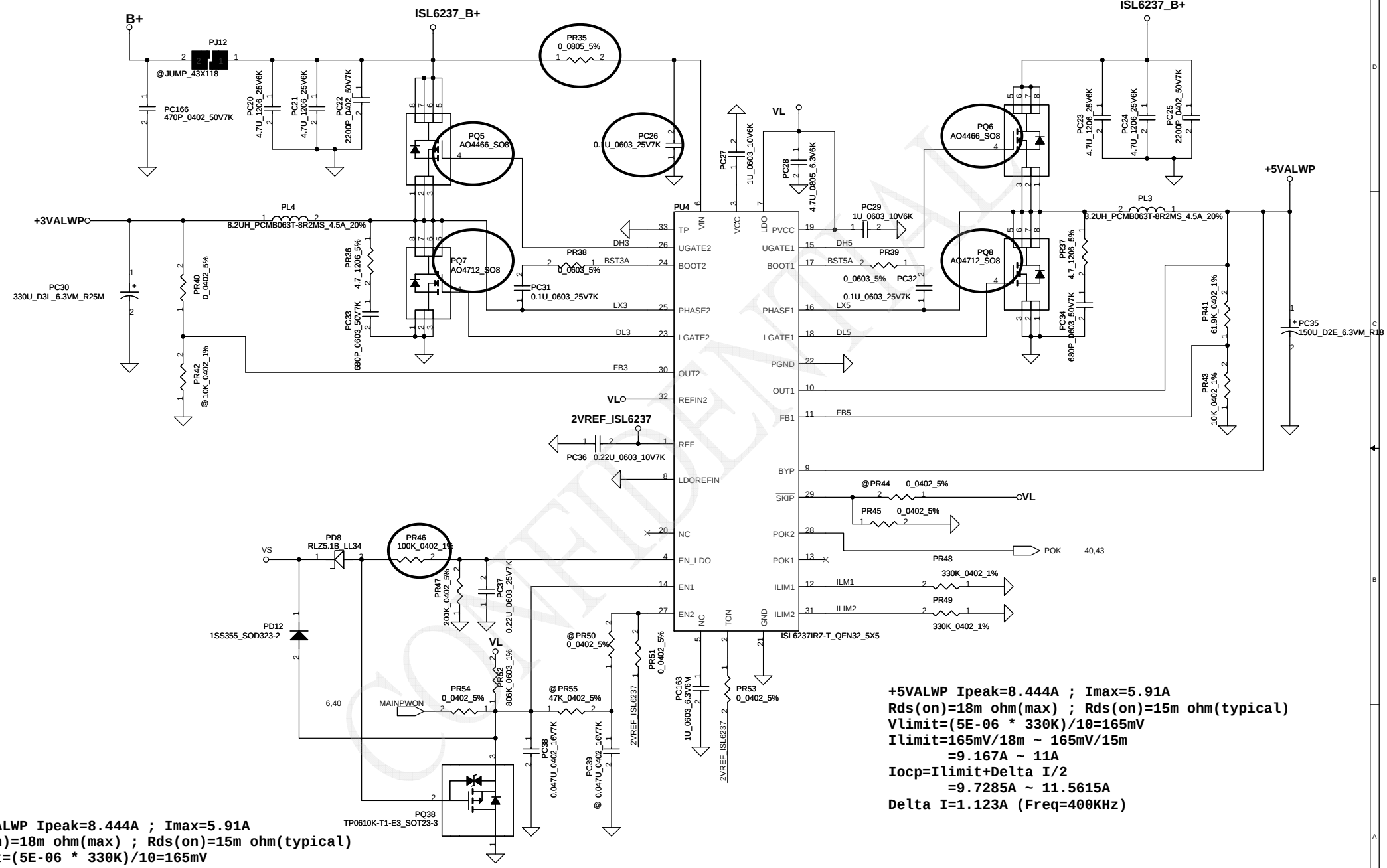

+5VALWP Ipeak=8.444A ; Imax=5.91A
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=9.7285A ~ 11.5615A
Delta I=1.123A (Freq=400KHz)

+3.3VALWP Ipeak=8.444A ; Imax=5.91A
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=9.721A ~ 11.554A
Delta I=1.108A (Freq=300KHz)

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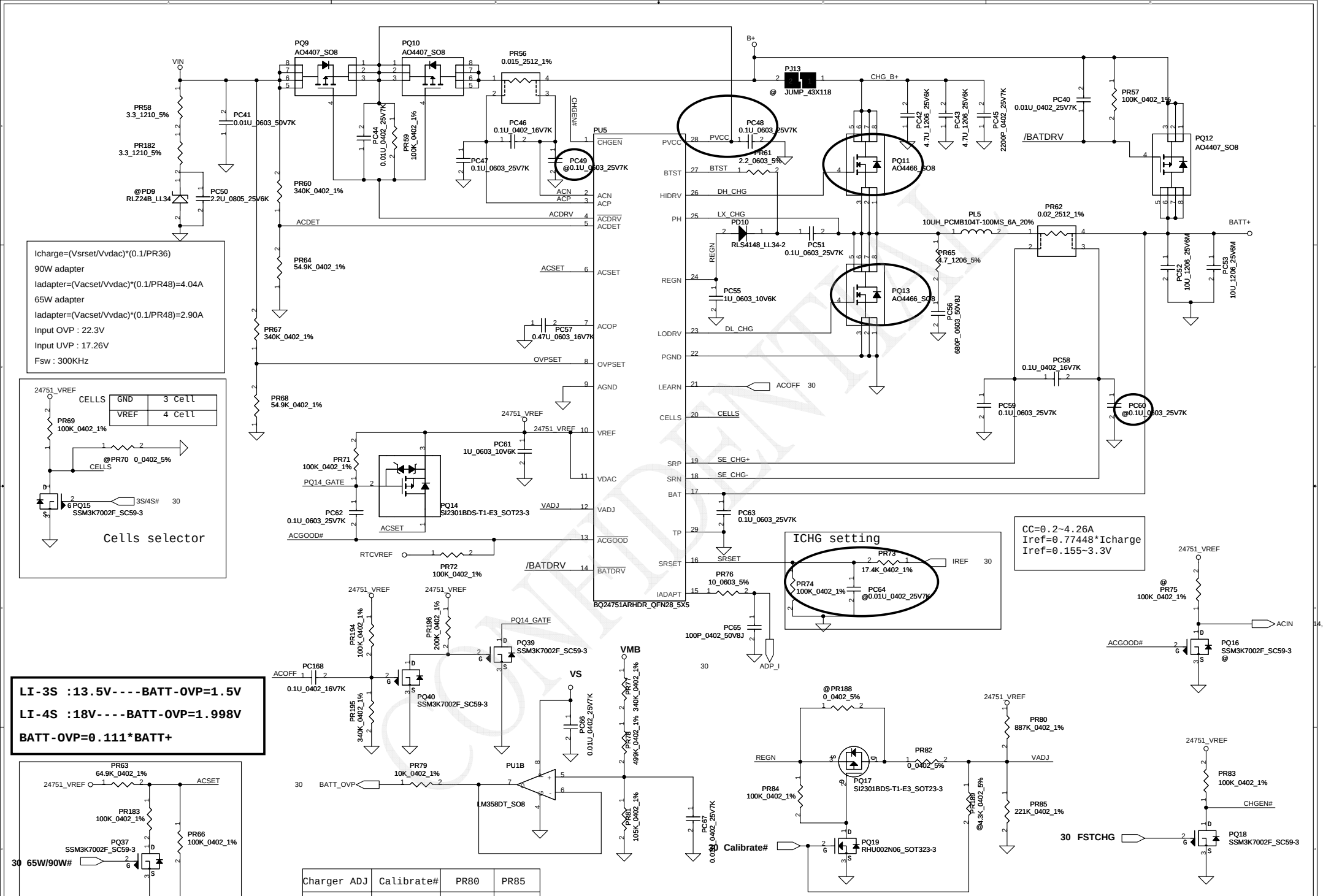

Icharge=(Vsrset/Vvdac)*(0.1/PR36)
90W adapter
Iadapter=(Vacset/Vvdac)*(0.1/PR48)=4.04A
65W adapter
Iadapter=(Vacset/Vvdac)*(0.1/PR48)=2.90A
Input OVP : 22.3V
Input UVP : 17.26V
Fsw : 300KHz

CELLS	
GND	3 Cell
VREF	4 Cell

LI-3S :13.5V----BATT-OVP=1.5V
LI-4S :18V----BATT-OVP=1.998V
BATT-OVP=0.111*BATT+

Charger ADJ	Calibrate#	PR80	PR85
4.0V	L	@	0
4.1V	L	887K	221K
4.2V	H	887K	221K

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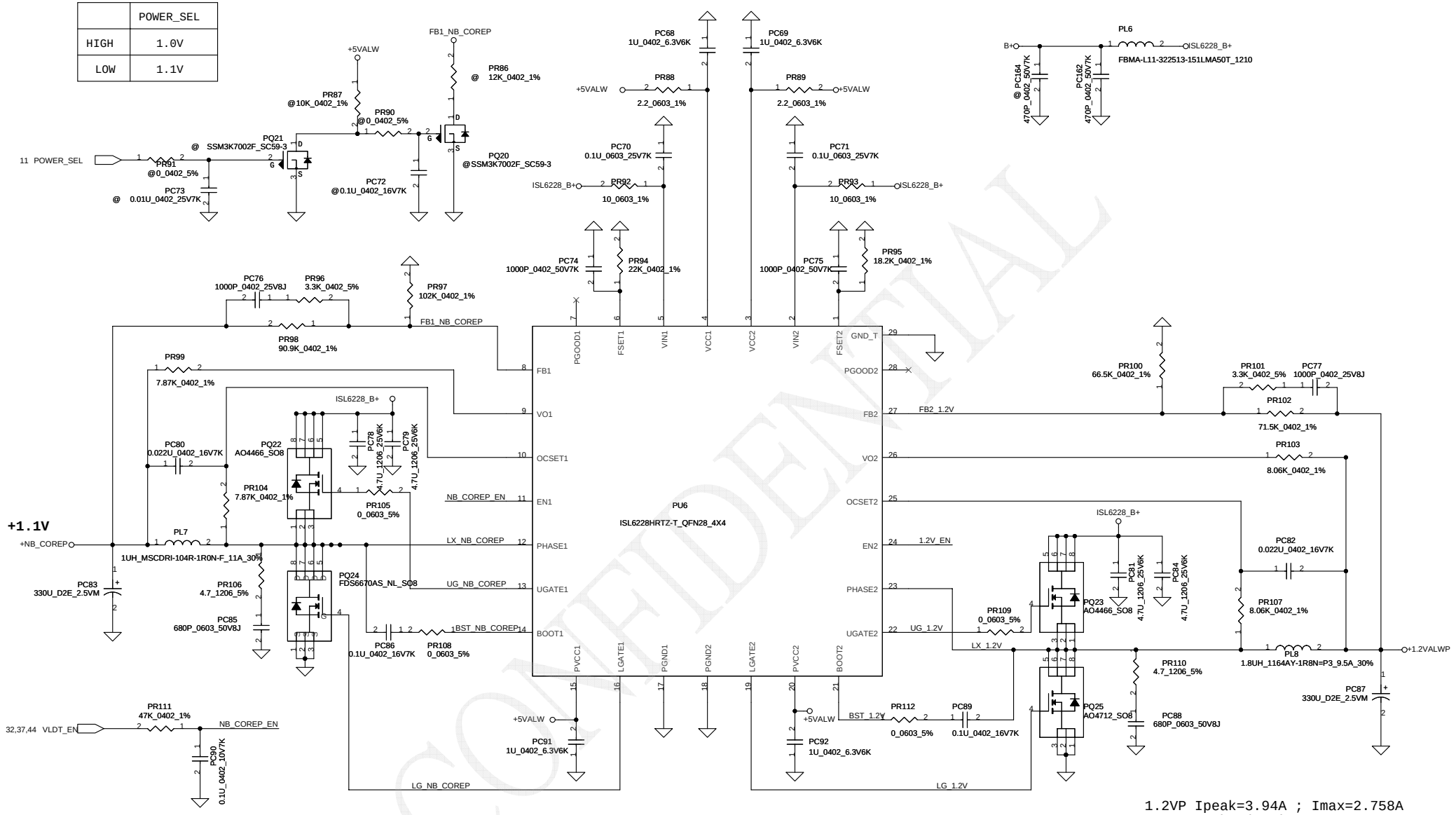
	POWER_SEL
HIGH	1.0V
LOW	1.1V



1.1VP Ipeak=8.9A ; Imax=6.23A
DCR=6m ohm (max)
Rocset=(Iocp*DCR)/10E-06=7.87K ohm
Iocp=10.09A(1.3*DCR)
Csen=L/(Rocset*DCR)=0.022uF

Freq=303KHz
Rfset=1/(1.5E-10 * Freq)=22K

1.2VP Ipeak=3.94A ; Imax=2.758A
DCR=10m ohm (max)
Rocset=(Iocp*DCR)/10E-06=6.65K ohm
Iocp=5.542A(1.2*DCR)
Csen=L/(Rocset*DCR)=0.027uF

Freq=366KHz
Rfset=1/(1.5E-10 * Freq)=18.2K

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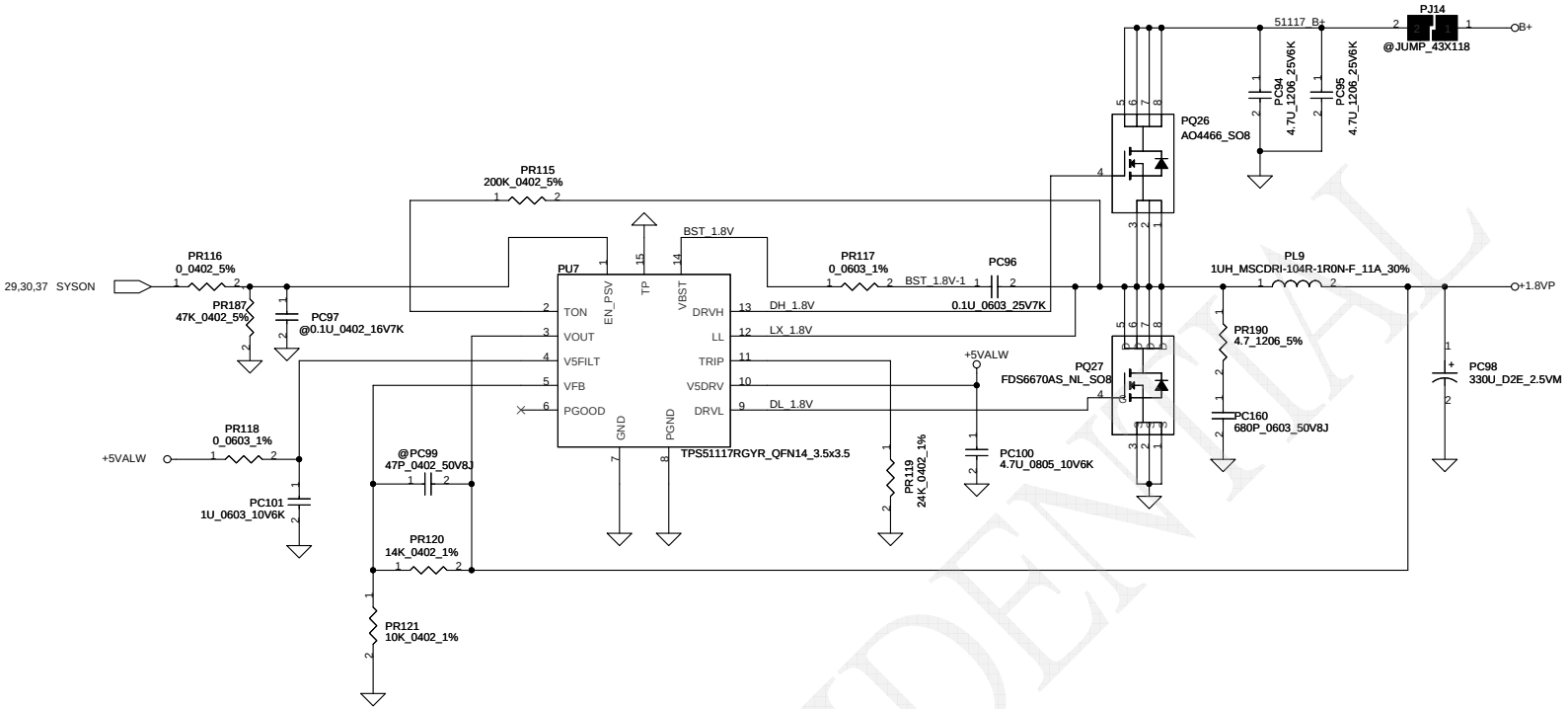
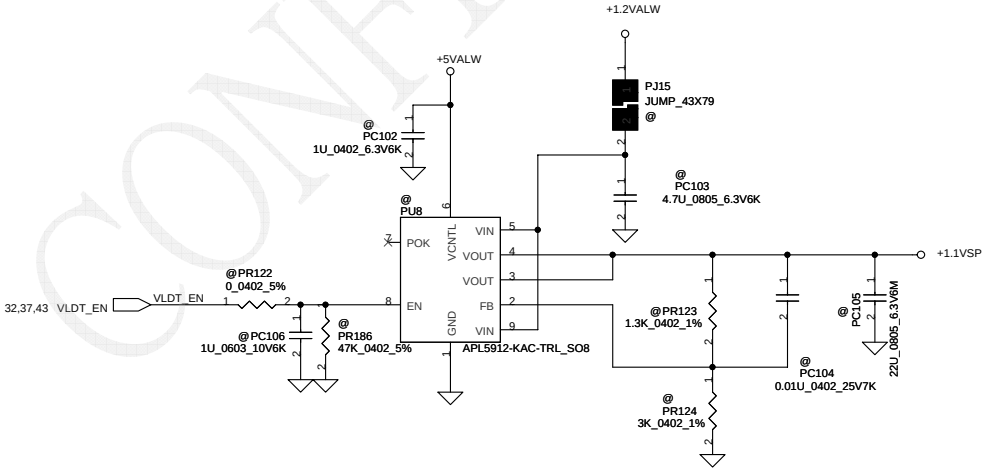


VFB=0.75V
Vo=VFB*(1+PR120/PR121)=1.8V
Ton=19E-12*Ron*(((2/3)*Vo+100mV)/Vin)+50ns=3.1E-07
Freq=305KHz

Cesr=15m ohm
Ipeak=12.6A Imax=8.82A
Delta I=((19-1.8)*(1.8/19))/(L*Freq)=5.332A
Vtrip=Rtrip*10uA=0.24V
Iocp-min=Vtrip/Rdsonmax*1.4+2.666=17.573A
Iocp-max=Vtrip/Rdsontyp*1.2+2.666=26.908A
Iocp=17.573~26.908A



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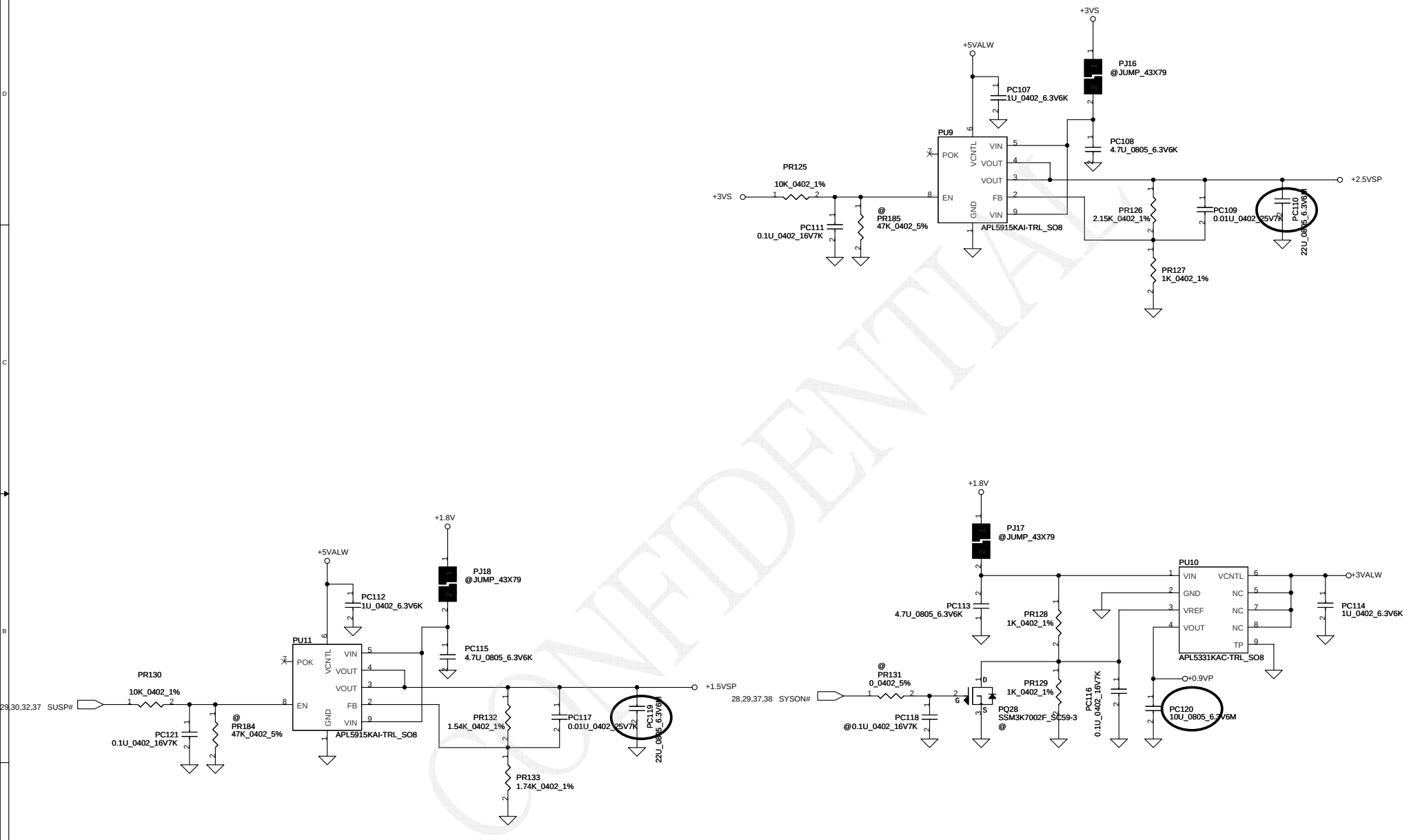

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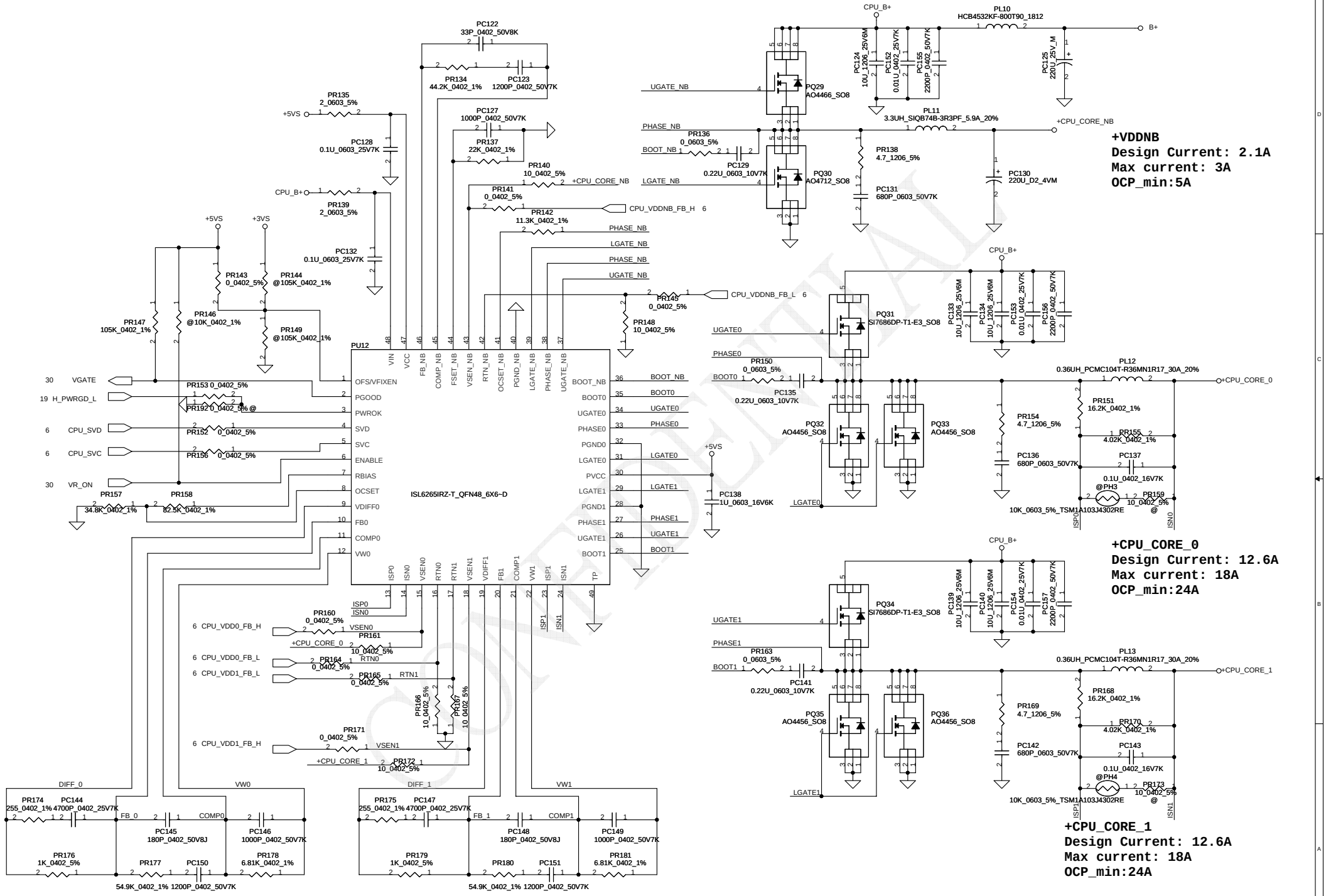

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	7/9	DCIN	Change PL1 to bead coil	link to SM010008E10
	7/9	DCIN	Link RTC battery symbol	link to SP093MX0000
	7/9	Battery conn	Change PL2 to bead coil	link to SM010008E10
	7/9	Battery conn	Change PD3,PD4 to RLS4148	For low cost
	7/9	Battery conn	Change PU2 pin8 to VL	Design change
	7/9	Charger	Delete PU3 PVCC resistor and change PC26 to 1U	avoid PQ6 false turn-on when AC plug-in
	7/9	Charger	Change PQ7,PQ9 to AO4466	For low cost
	7/9	Charger	Change PU4 pin8 to +5VALW	Design change
	7/9	Charger	Unpop PC28, PC37	avoid interfere by other signal
	7/9	3V/5V	Change PR54 and PC51	Add design margine
	7/9	3V/5V	Change MOSFET to AO4466+AO4712	For low cost
	7/9	1.8V/1.5V	Change MOSFET to AO4466+AO4712	For low cost
	7/9	1.8V/1.5V	Change PR75 to 2.2ohm	Design change
	7/9	1.05V/1.25V/0.9V	Change MOSFET to AO4466+AO4712	For low cost
	7/9	1.05V/1.25V/0.9V	Change PC94 to 330U	Decrease overshoot
	7/9	1.05V/1.25V/0.9V	Change PU7 PVCC source to +5VS	Design change
	7/9	1.05V/1.25V/0.9V	Change PC105,PC108 size to 0805	For low cost
	7/9	CPU CORE	Change input MLCC to 4pcs	Design change
	7/9	CPU CORE	Unpop PC111	Reserve for high frequency noise
	7/10	Charger	Change PR38, PR39 and unpop PC32	increase resistor to reduce power loss on resistor divider
	7/10	Charger	Change PR45, PR47 and unpop PC41	increase resistor to reduce power loss on resistor divider
	7/10	Charger	Change PR43 to 100K	increase resistor to reduce power loss
	7/10	3V/5V	Change PR65 to 100K_1%	Let BOM clear
	7/10	Charger/0.9V	Change PQ4,PQ11,PQ12,PQ13,PQ24 to SB000009080	For low cost
	8/1	Charger	Change PR30 to 0.015ohm and PR38 to 80.6K	Change over power protection point

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	12/11	p.11	DEL R26	
	12/11	P.15	UN-POP R234,POP R235	
	12/11	P.17	Change R123 to 2.2K	
	12/11	P.18	ADD R525,R526,R527	For non-Dockin sku
	12/11	P.20	Del R128	
	12/11	P.23	Change R103 to 2.2k	
	12/11	P.25	DEL U35,Q43,R473	
	12/11	P.27	ADD RP32,RP33,RP34,RP35,RP36	For non-Dockin sku
	12/11	P.29	Change U17 P/N to SA000029E00	
	12/11	P.31	Change JP14.4 Net to EC_SMB_CK2,JP14.5 Net to EC_SMB_DA2	
	12/11	P.31	Change LED1,LED2 P/N to SC597UDB000	
	12/11	P.35	Change U40.3 to WOOFER_IN+,U40,4 to WOOFER_IN-	
	12/11	P.38	Del R291,R292	
	12/14	P.30	Raise KB926 pin.75	
	12/12	P.14	ADD D28 and pull high R529 to +3VS to AC_IN form JMXM1.157	
	12/12	P.17	Change Q47,Q48,Q49,Q50 P/N to SB501110010	
	12/12	P.18	DEL Q5,ADD Q52,Q53	
	12/12	P.33	Change U31 P/N to SA000026V00	
	12/12	P.30	Change Board ID	
	12/12	P.26	Un-pop R56, POP R61	
	12/13	P.25	DEL U35,R473,Q43	
	12/13	P.7	DEL C762,C763	
	12/14	P.38	update dock footprint and add CRT_Det#	
	12/19	P.18	change CRT_DET to CRT_DET# from CRT to Q36 and output CRT_DET TO U10.J2	
	12/14	P.26	DEL U23,R305,C399,R28	
	12/14	P.6	Change R420, R419, R113 pull-up change to +1.8VS	
	12/14	P.12	Delete U6, R68, R65, Q6, R55, C119, C113, C128, C151,C124	Remove 1.35V LDO circuit
	12/14	P.12	Del L22, POP L21	Change VDDHTTX from 1.35V to 1.2V
	12/14	P.14	Change C183 to 0402 package	
	12/14	P.16	Change C12 to 0402 package	
	12/14	P.17	Change R90,R91 from 1.5K to 2K	
	12/14	P.22	Delete R399, add R391	VDD should connect to S0 power on A12
	12/14	P.34	Change R480, R487 from 0Ohm to 75Ohm	
	12/14	P.37	Change R306 to 10K	
	12/14	P.32	Change D16.1 from +3VS to SUSP#	1.2V_HT should faster than NB_CORE
	12/19	P.25	Connect U33.16 to U10.AD18 (CR_WAKE#) through D29; U33.13 to U10.F2 (CR_PE#) through a MOS(Q55)	VGA_ON should drop before +3VS
	12/17	P.28	DEL TV_THERM#,ADD Port80 Signal to JMINI2.49,JMINI2.51	
	12/17	P.19	Delete R179,R185, add U12, U13	

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	12/17	P.26	Del BCM5787 Co-lay part	
	12/17	P.38	ADD EC_DOCKIN#_S0	
	12/18	P.25	ADD R533	
	12/19	P.11	ADD Q54,R534 Level shift, and CPU_LDT_REQ#,ALLOW_LDTSTOP Pull high 300 to 1.8vs	
	12/19	P.20	Change New Card CP_PE# to SB GPM5#	
			Change CRT_DET to SB GPM7#	
			Change EC_LID_OUT# to SB GPM4#	
			Del USB_OC#4	
	12/19	P.6	ADD R129,R538,R539	
	12/19	P.21	change R104 from 10K to 100K	
	12/19	P.34	Change R488,R483 to 75 ohm	
	12/19	P.37	Change R306 from 10K to 150K	
	12/19	P.6	POP R93	
	12/19	P.18	change D18 from RB411 to RB491	
	12/19	P.19	Change Y2 location to X2 and p/n change to SJ132P7K220	
	12/19	P.30	EC_SMB_CK1,EC_SMB_DA1 Pull high to +3VALW,EC_SMB_CK2,EC_SMB_CK2 pull high to +3VS	
	12/20	P.37	Reserve R541,R542,R543	
	12/20	P.33	Change R294,R288 P/N to SM010016720	
	12/20	P.31	ADD C655,C656,C657,C658,C659,C660,C661,C662 for EMI	
	12/20	P.37	ADD Q57,R544	
	12/20	P.34	JMIC1.7,JMIC1.8,JLINE1.7,JLINE1.8 connect to AGND,	
	12/21	P.21	Change SATA HDD Port to U10 SATA port 1	
	12/24	P.21/P22.	Change D7,D9 P/N to SC1B751V010	
	12/24	P.34	Change L73,L74,L67,L68,L71,L72 P/N to SM010015410	
	12/24	P.21	ADD SPI ROM Schematic for SB700	
	12/24	P.34	JHP1.6,JHP1.10 connect to AGND	
	12/24	P.29	Add U17 .21 to gnd	
	12/24	P.26	Change U5.18,U5.17,U5.5,U5.33 connect to +1.2_VDDCIO	
	12/26	P.34	Change R490 to 42.2K, R478,R479 to 1K,C621,C622 to 0.22u	
	12/26	P.35	Change R516 to 6.8K	
	1/22	P.15	Reversal MiniCard1 & MiniCard2 PCIE CLK Signal	
	1/22	P.37	Change R275 from 100K to 10K	
	1/22	P.37	Change Q57.2 to VLDT_EN#	
	1/31	P.6	POP CPU internal themal sensor schematic	
	1/31	P.11	change R64 to 133 ohm	
	1/31	P.14	Add AND GATE	
	1/31	P.15	Add C669	
	1/31	P.17	Change EC_DOCKIN#_S0 to Q50.2/Q49.2	
	1/31	P.18	Change EC_DOCKIN#_S0 to U7.1	
	1/31	P.20	Change CRT_DET to U10.H7,add EC_DOCKIN# to U10.B9	

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	1/31	P.21	Reserve AND gate form ACIN to U10.A4	
	1/31	P.28	Reserve MINI1_LED# Pull high 100K to +3VS	
	1/31	P.30	ADD R551,R552 (VR_ON pull down 100k,BT_ON# Pull 100k)	
	1/31	P.30	Del JP12	
	1/31	P.33	Change R257 from 200k to 330k	
	1/31	P.33	ADD EC_DOCKIN#_S0 to R530.1	
	1/31	P.34	Change R459,R446,R475,R470 to 75ohm	
	1/31	P.34	Add R553,R554,R555,R556	
	1/31	P.38	Add C672	
	2/4	P.25	For EMI request,add C676	
	2/4	P.31	For EMI request,add C673,C674,C675	
	2/4	P.34	For EMI request,add D31	
	2/12	P.6	Change R361,R365 to 2.2k	
	2/12	P.30/31	ADD ESB_CLK/ESB/DATA (add R557,R558,R559,R560,R561,R562)	
	2/13	P.28	ADD R563	
	2/14	P.6/20	UPDATE cpu internal themal sensor schematic (add R564,R565,R566,R567,R568,R569,ADD CPU_SIC_SB,CPU_SID_SB)	
	3/12		R493=>61.9K (SD034619280) R516=>1K (SD028100180) R517=>4.7K (SD028470180) R518=>1.8K (SD028180180) C647=> 0.068u (SE026683K80)	
	3/12	P.33	For EMI request,Change R440 to SD028100A80	
	3/12	P.12	Change C109,C150,C130,C88,C92,C35,C34,C36,C38 to SE000000I10 (22U)	
	3/12	P.7	Change C77,C78,C79,C80 to SGA00002380	
	3/12	P.37	Change R186 to10K	
	3/17	P.11	ADD R570,R571, Un-pop Q28,Q56,R324,R534	
	3/26	P.6	Un-pop R351,C436,R360,R566,R568,Q31,Q30	
	3/26	P.19	Change C192,C22 to 22p	
	3/26	P.34	Change R487,R480,R488,R483 to 56.2	
	4/16	P.8	Change C257 from 0.1U to 1UF	
	4/16	P.19	Change C192, C212 to 12P for RTC Timer issue	
	4/16	P.28	Add L, C on SYSON# signal close to USB/B connector and TV/B connector	
	4/16	P.30	Change the board ID back to R0.3 for BIOS identify issue	
	4/16	P.31	Add 100pF capacitor on +3VS close to MEDIA/B	
	4/16	P.32	Change C373 to 0.22U_0603_X7R for VGA power sequence	
	4/16	P.32	Remove power on/off button SW3 for MP BOM	
	4/16	P.37	Reserve voltage divider circuit on Power MOS	
	4/23	P.31	change R285,R286 resistor value to 300 ohm	
	4/23	P.31	change R284,R287 resistor value to 453 ohm	
	4/30	P.30	change R216,R217 resistor value to 2.2k ohm	
	5/20	P.22	Add R578	
	5/20	P.24	Add C681,C682	

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